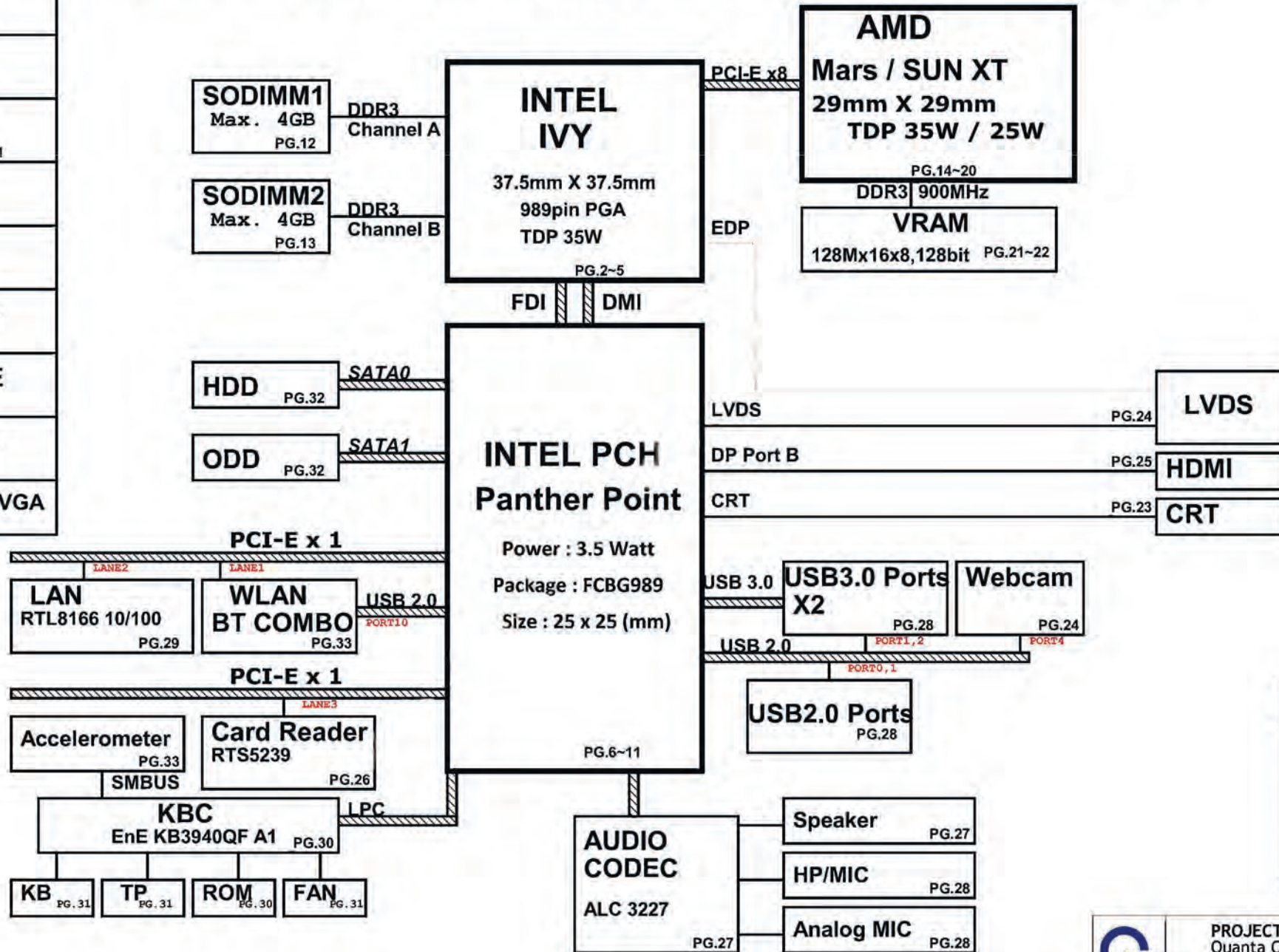
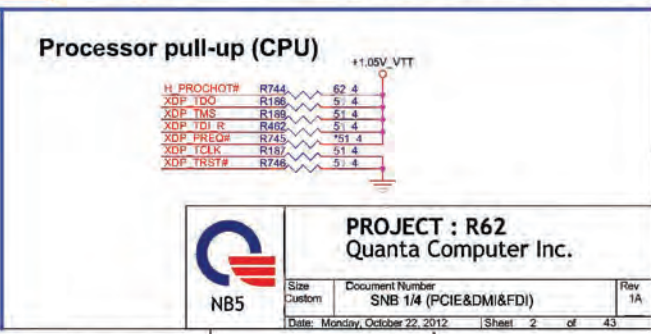
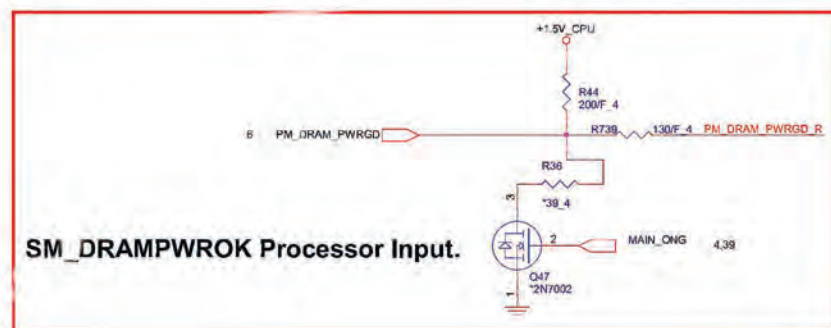
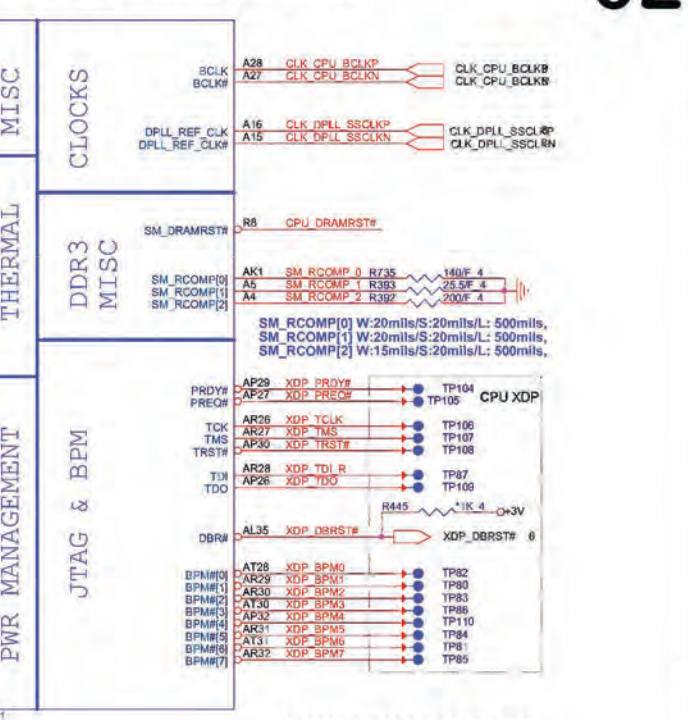


R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

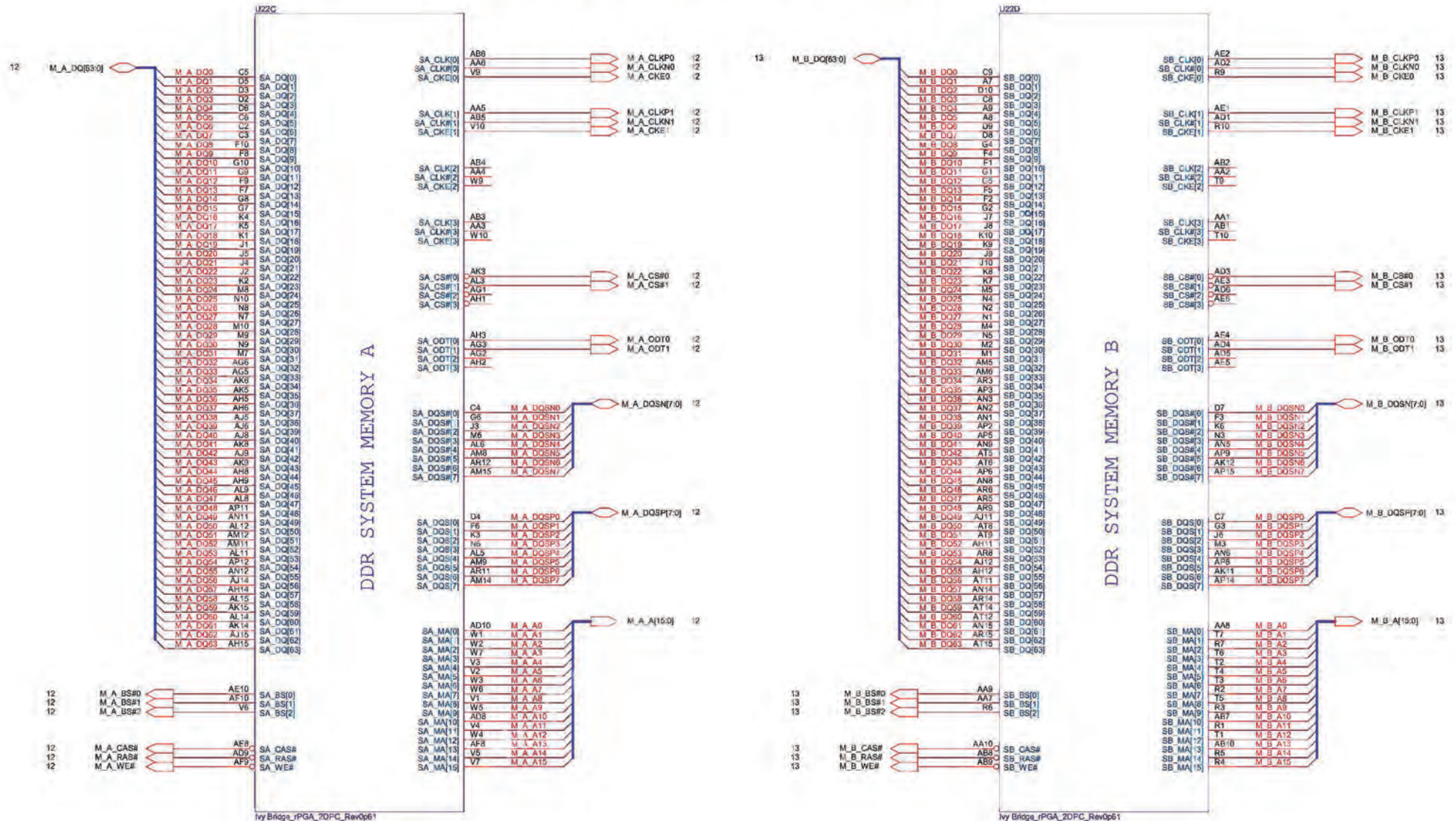
01

+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43





Ivy Bridge Processor (DDR3)



PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number SNB 2/4 (DDR3 I/F)	Rev 1A
Date: Monday, October 22, 2012	Sheet 3 of 43	

Ivy Bridge Processor (POWER)

POWER

U22F

SNB: 55A

+VCC_CORE

IVY: 55A

VCC1

VCC2

VCC3

VCC4

VCC5

VCC6

VCC7

VCC8

VCC9

VCC10

VCC11

VCC12

VCC13

VCC14

VCC15

VCC16

VCC17

VCC18

VCC19

VCC20

VCC21

VCC22

VCC23

VCC24

VCC25

VCC26

VCC27

VCC28

VCC29

VCC30

VCC31

VCC32

VCC33

VCC34

VCC35

VCC36

VCC37

VCC38

VCC39

VCC40

VCC41

VCC42

VCC43

VCC44

VCC45

VCC46

VCC47

VCC48

VCC49

VCC50

VCC51

VCC52

VCC53

VCC54

VCC55

VCC56

VCC57

VCC58

VCC59

VCC60

VCC61

VCC62

VCC63

VCC64

VCC65

VCC66

VCC67

VCC68

VCC69

VCC70

VCC71

VCC72

VCC73

VCC74

VCC75

VCC76

VCC77

VCC78

VCC79

VCC80

VCC81

VCC82

VCC83

VCC84

VCC85

VCC86

VCC87

VCC88

VCC89

VCC90

VCC91

VCC92

VCC93

VCC94

VCC95

VCC96

VCC97

VCC98

VCC99

VCC100

Ivy Bridge_rPGA_2DPC_Rev0p61

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

SNB: 8.5A

IVY: 8.5A

+1.05V_VTT

VCC101

VCC102

VCC103

VCC104

VCC105

VCC106

VCC107

VCC108

VCC109

VCC110

VCC111

VCC112

VCC113

VCC114

VCC115

VCC116

VCC117

VCC118

VCC119

VCC120

VCC121

VCC122

VCC123

VCC124

VCC125

VCC126

VCC127

VCC128

VCC129

VCC130

VCC131

VCC132

VCC133

VCC134

VCC135

VCC136

VCC137

VCC138

VCC139

VCC140

VCC141

VCC142

VCC143

VCC144

VCC145

VCC146

VCC147

VCC148

VCC149

VCC150

VCC151

VCC152

VCC153

VCC154

VCC155

VCC156

VCC157

VCC158

VCC159

VCC160

VCC161

VCC162

VCC163

VCC164

VCC165

VCC166

VCC167

VCC168

VCC169

VCC170

VCC171

VCC172

VCC173

VCC174

VCC175

VCC176

VCC177

VCC178

VCC179

VCC180

VCC181

VCC182

VCC183

VCC184

VCC185

VCC186

VCC187

VCC188

VCC189

VCC190

VCC191

VCC192

VCC193

VCC194

VCC195

VCC196

VCC197

VCC198

VCC199

VCC200

VCC201

VCC202

VCC203

VCC204

VCC205

VCC206

VCC207

VCC208

VCC209

VCC210

VCC211

VCC212

VCC213

VCC214

VCC215

VCC216

VCC217

VCC218

VCC219

VCC220

VCC221

VCC222

VCC223

VCC224

VCC225

VCC226

VCC227

VCC228

VCC229

VCC230

VCC231

VCC232

VCC233

VCC234

VCC235

VCC236

VCC237

VCC238

VCC239

VCC240

VCC241

VCC242

VCC243

VCC244

VCC245

VCC246

VCC247

VCC248

VCC249

VCC250

VCC251

VCC252

VCC253

VCC254

VCC255

VCC256

VCC257

VCC258

VCC259

VCC260

VCC261

VCC262

VCC263

VCC264

VCC265

VCC266

VCC267

VCC268

VCC269

VCC270

VCC271

VCC272

VCC273

VCC274

VCC275

VCC276

VCC277

VCC278

VCC279

VCC280

VCC281

VCC282

VCC283

VCC284

VCC285

VCC286

VCC287

VCC288

VCC289

VCC290

VCC291

VCC292

VCC293

VCC294

VCC295

VCC296

VCC297

VCC298

VCC299

VCC300

VCC301

VCC302

VCC303

VCC304

VCC305

VCC306

VCC307

VCC308

VCC309

VCC310

VCC311

VCC312

VCC313

VCC314

VCC315

VCC316

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VCC322

VCC323

VCC324

VCC325

VCC326

VCC327

VCC328

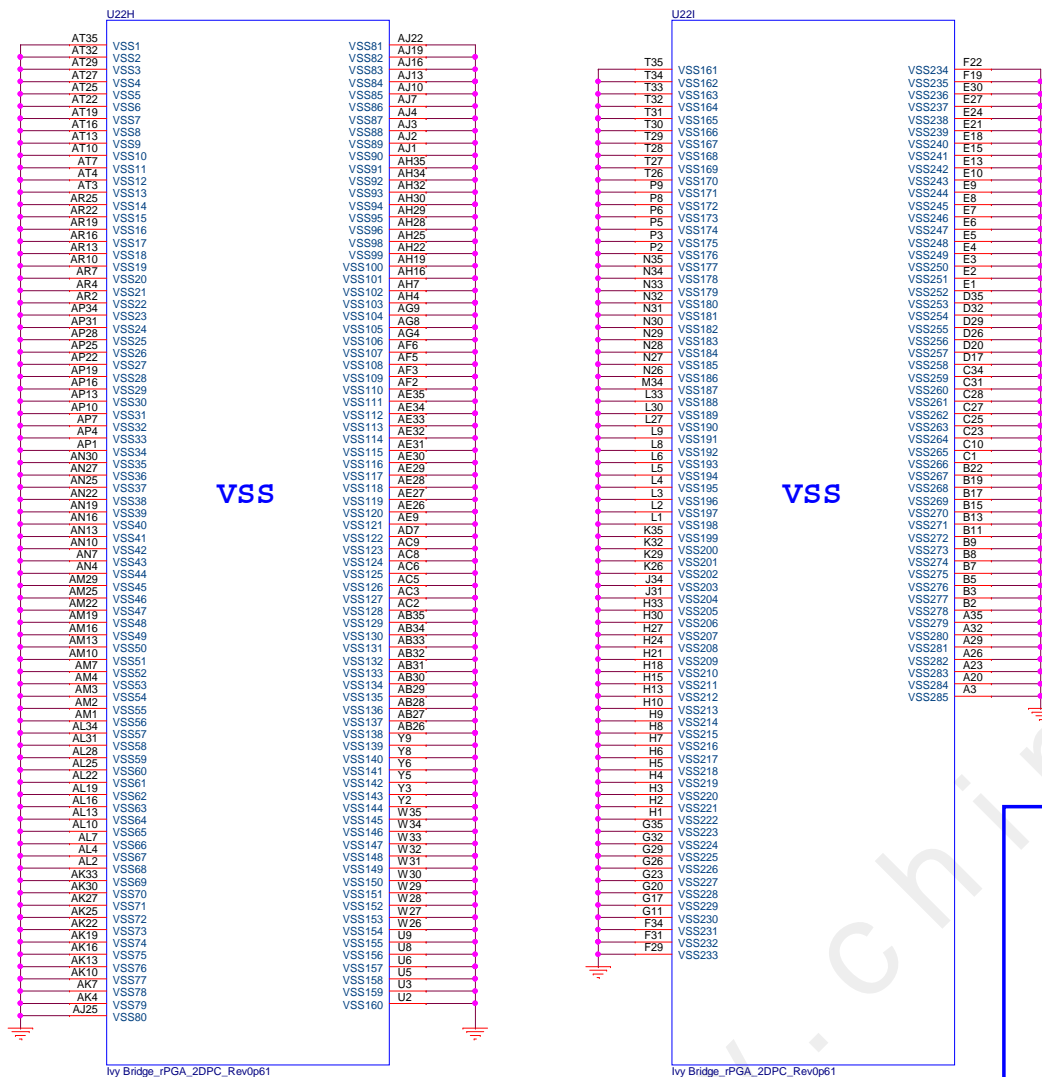
VCC329

VCC330

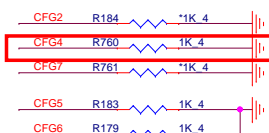
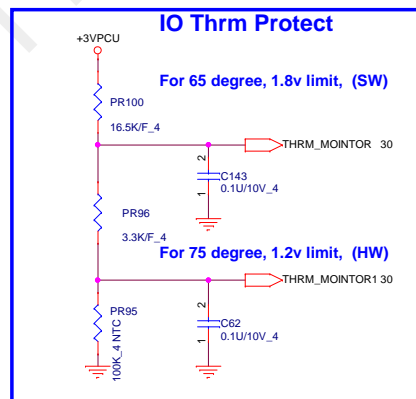
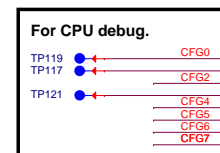
VCC331

VCC332

Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

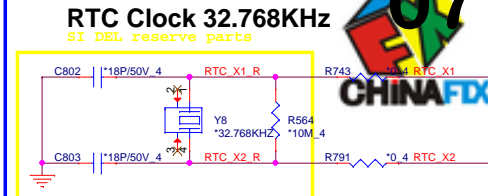
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP Enable; An ext DP device is connected to eDP	
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

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Quanta Computer Inc.

Size Custom Document Number SNB 4/4 (GND) Rev 1A

Date: Monday, October 22, 2012 Sheet 5 of 43

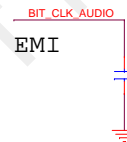
07



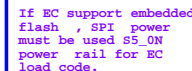
30mils



PCH JTAG Debug(CLG)











+SPI_PWR

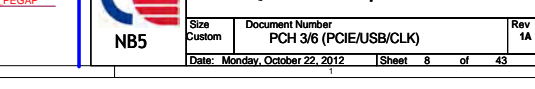
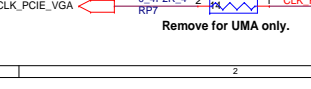
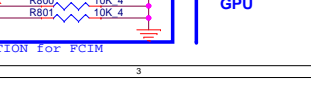


NB5

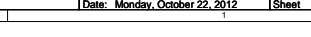
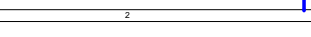
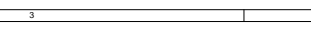
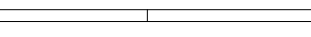
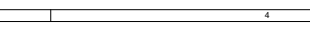
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
Date: Monday, October 22, 2012	Sheet 7 of 43	

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <i>Different from Calpella</i>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V0 									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security <i>Only for Interposer</i>	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	0	0	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# 
GNT1#	GNT0#	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19 <i>Different from Calpella</i>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection <i>Only for Interposer</i>	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V0 									
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V0 									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO 									
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overriden	GPIO33_E 									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <i>Different from Calpella</i>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPL_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

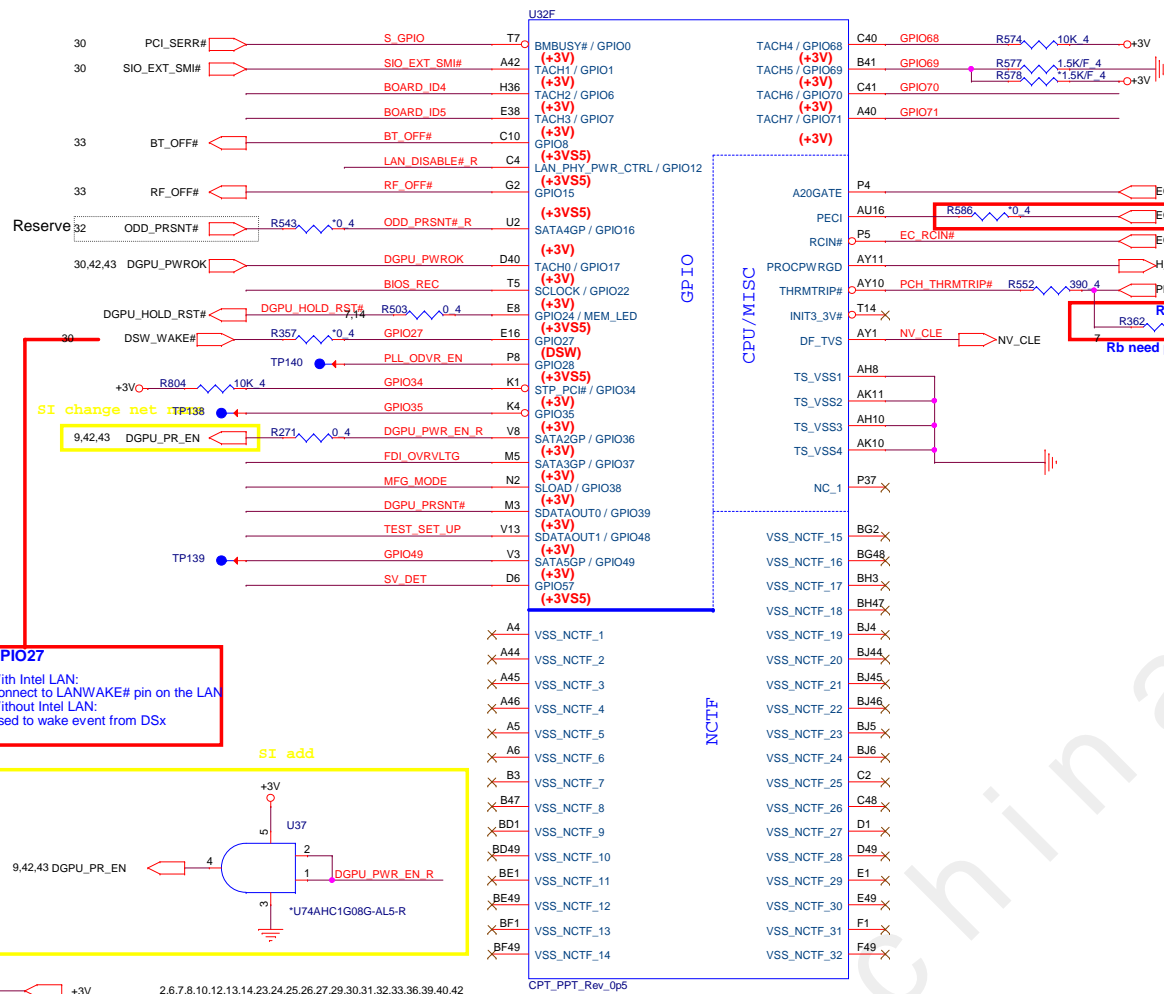
5



5



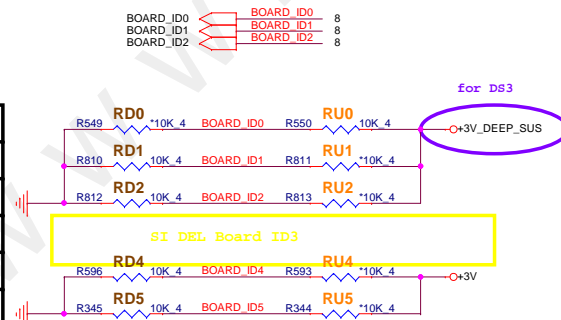
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



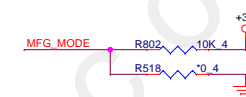
BOARD ID SETTING

BOARD_ID1
For Stage Use

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
				0	1	1
				1	1	1
				0	0	0

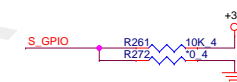


MFG-TEST



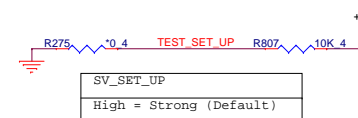
Swap GPIO

0 = SC
1 = De

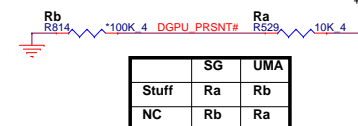
for l

ME Crypto Transport Layer
ity (TLS) cipher suite

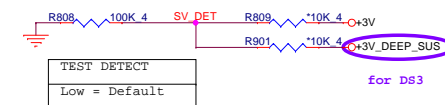
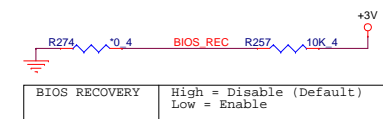
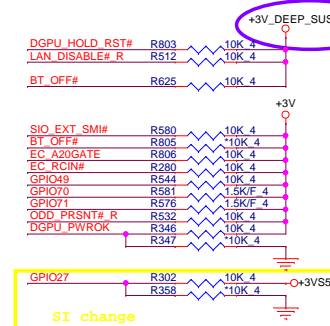
Disable (Default)
= Enable



GFX Present



GPIO Pull-up/Pull-down(CLG) for DS3



PROJECT : R62
Quanta Computer Inc.

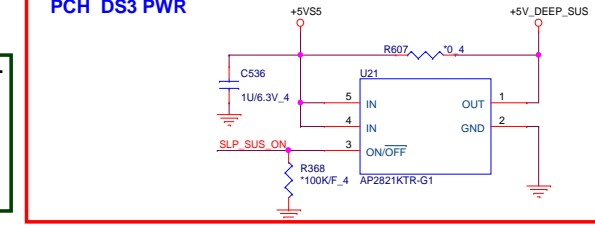
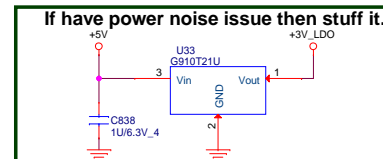
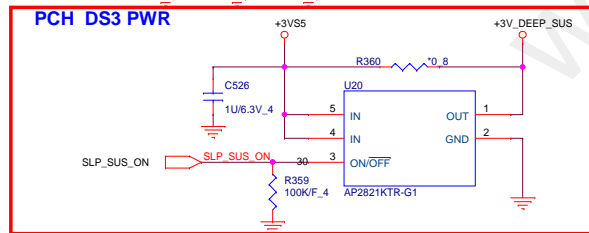
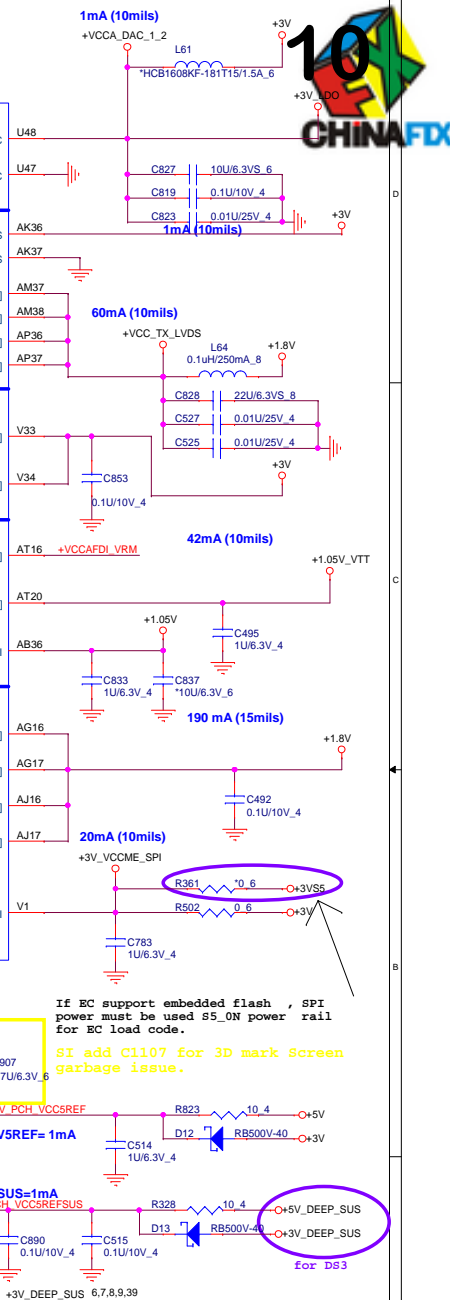
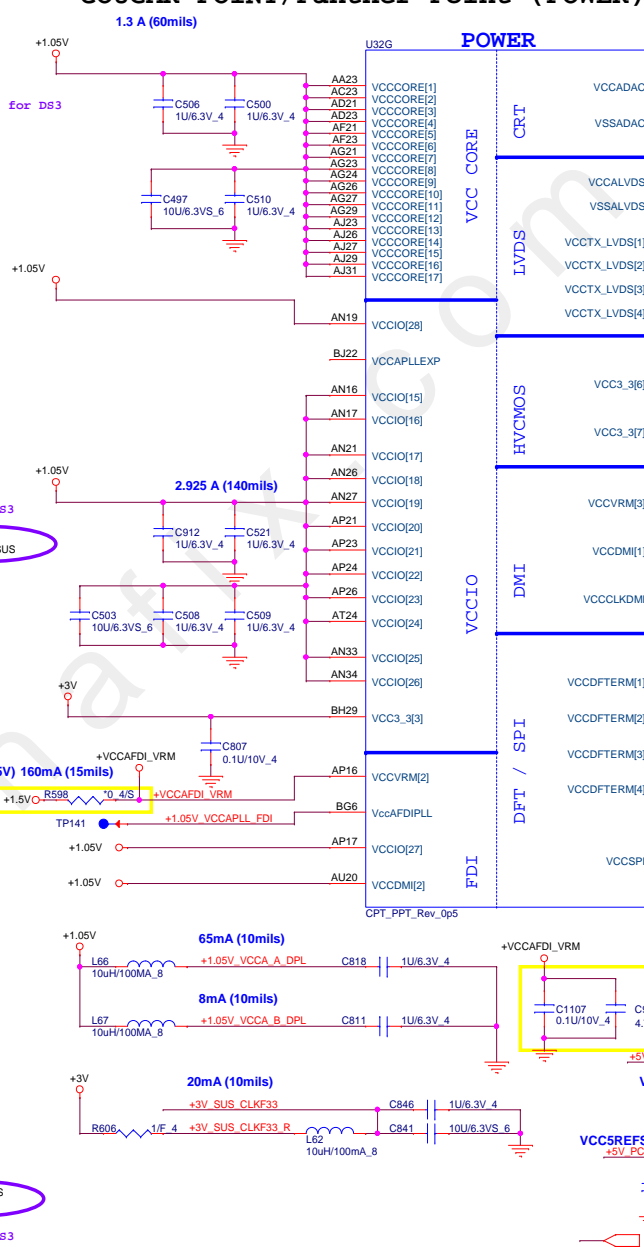
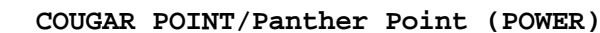
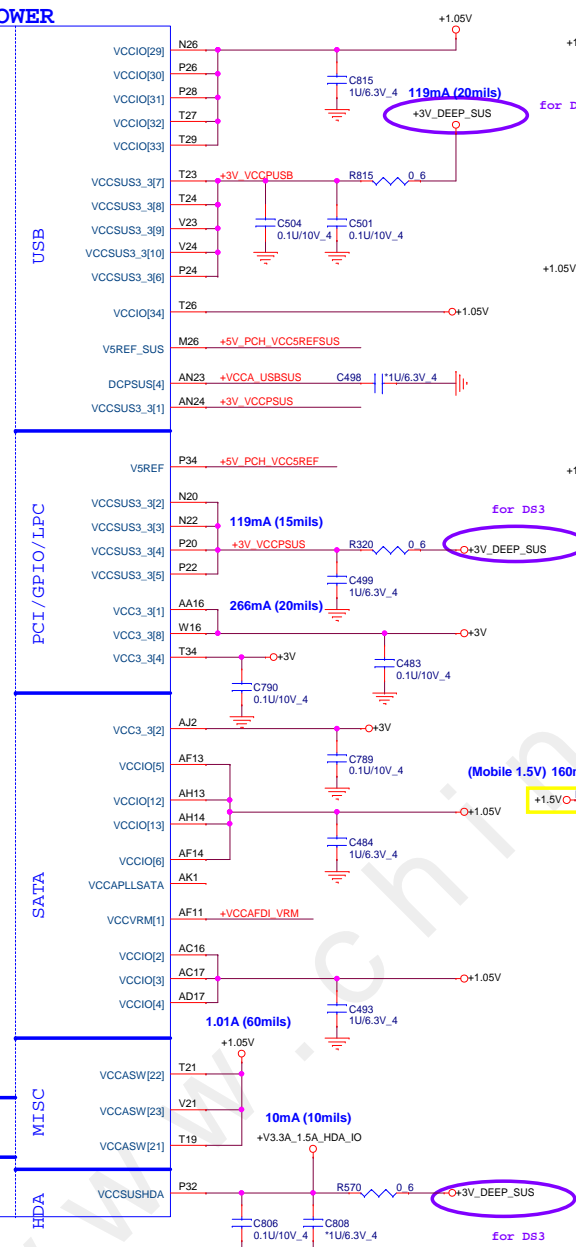
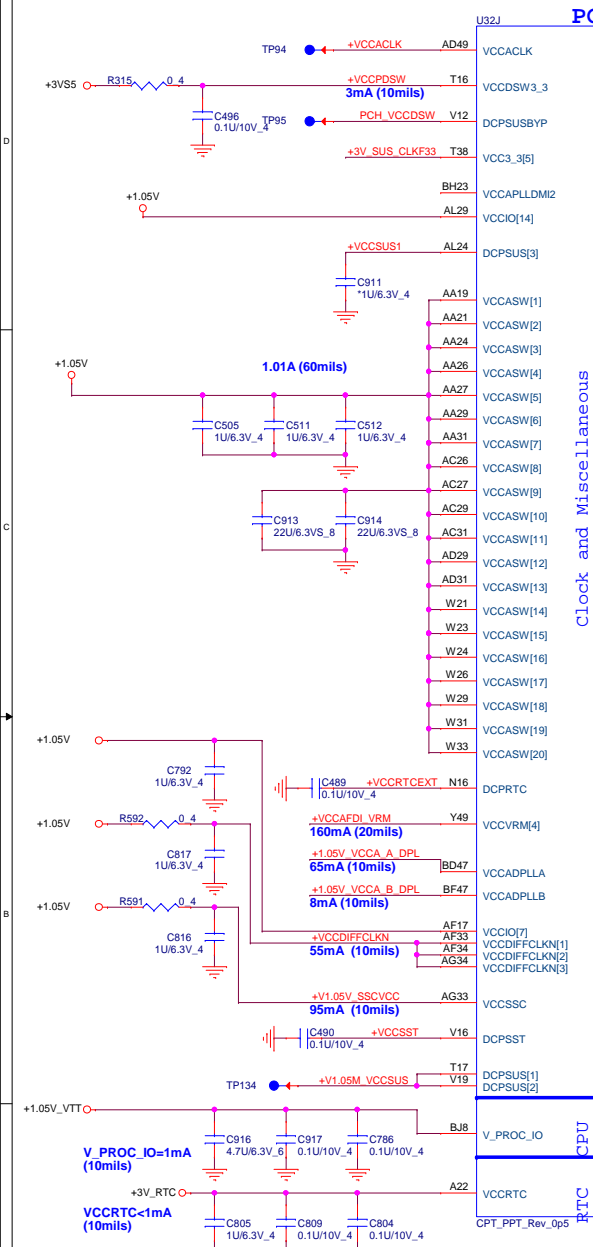
Size	Document Number
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Size	Document Number
Custom	PCH 4/6 (GPIO/MISC)

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Rev

Cougar Point/Panther Point (POWER)



 NB5	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
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Cougar Point/Panther Point (GND)

AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	L18
B19	VSS[165]	L2
B23	VSS[166]	L20
B27	VSS[167]	L26
B31	VSS[168]	L28
B35	VSS[169]	L36
B39	VSS[170]	L48
B7	VSS[171]	M12
F45	VSS[172]	M18
BB12	VSS[173]	M22
BB16	VSS[174]	M24
BB20	VSS[175]	M30
BB22	VSS[176]	M32
BB24	VSS[177]	M34
BB28	VSS[178]	M38
BB30	VSS[179]	M4
BB38	VSS[180]	M42
BB4	VSS[181]	M46
BB46	VSS[182]	M8
BC14	VSS[183]	N18
BC18	VSS[184]	N30
BC2	VSS[185]	N47
BC22	VSS[186]	P11
BC26	VSS[187]	P18
BC32	VSS[188]	P30
BC34	VSS[189]	P43
BC36	VSS[190]	P47
BC40	VSS[191]	P7
BC42	VSS[192]	R2
BD46	VSS[193]	R48
BD5	VSS[194]	T12
BE22	VSS[195]	T31
BE26	VSS[196]	T4
BE40	VSS[197]	W34
BF10	VSS[198]	T46
BF12	VSS[199]	V36
BF16	VSS[200]	V39
BF20	VSS[201]	V43
BF22	VSS[202]	V7
BF24	VSS[203]	W17
BF26	VSS[204]	W19
BF28	VSS[205]	W2
BD3	VSS[206]	W27
BF30	VSS[207]	W48
BF38	VSS[208]	Y12
BF40	VSS[209]	Y38
BF8	VSS[210]	Y4
BG17	VSS[211]	Y42
BG21	VSS[212]	Y46
BG33	VSS[213]	Y8
BG44	VSS[214]	BG29
BG8	VSS[215]	N24
BH11	VSS[216]	AJ3
BH15	VSS[217]	AD47
BH17	VSS[218]	B43
BH19	VSS[219]	BE10
H10	VSS[220]	BG41
BH27	VSS[221]	G14
BH31	VSS[222]	H16
BH33	VSS[223]	T36
BH35	VSS[224]	BG22
BH39	VSS[225]	BG24
BH43	VSS[226]	C25
BH7	VSS[227]	AP13
D3	VSS[228]	M14
D12	VSS[229]	AP3
D16	VSS[230]	AP1
D18	VSS[231]	BE16
D22	VSS[232]	BC16
D24	VSS[233]	BG28
D26	VSS[234]	BJ28
D28	VSS[235]	
D30	VSS[236]	
D32	VSS[237]	
D34	VSS[238]	
D38	VSS[239]	
D42	VSS[240]	
D8	VSS[241]	
E18	VSS[242]	
E26	VSS[243]	
G18	VSS[244]	
G20	VSS[245]	
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

U32I

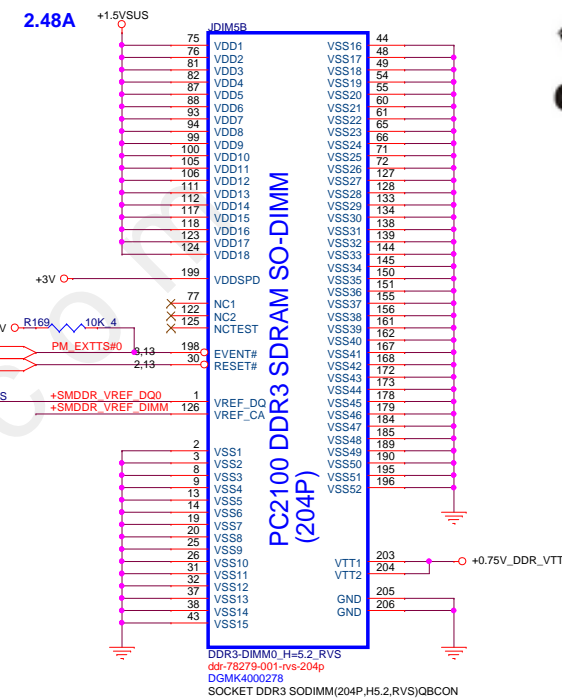
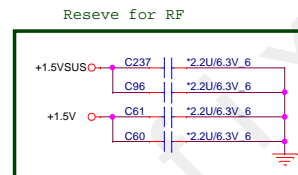
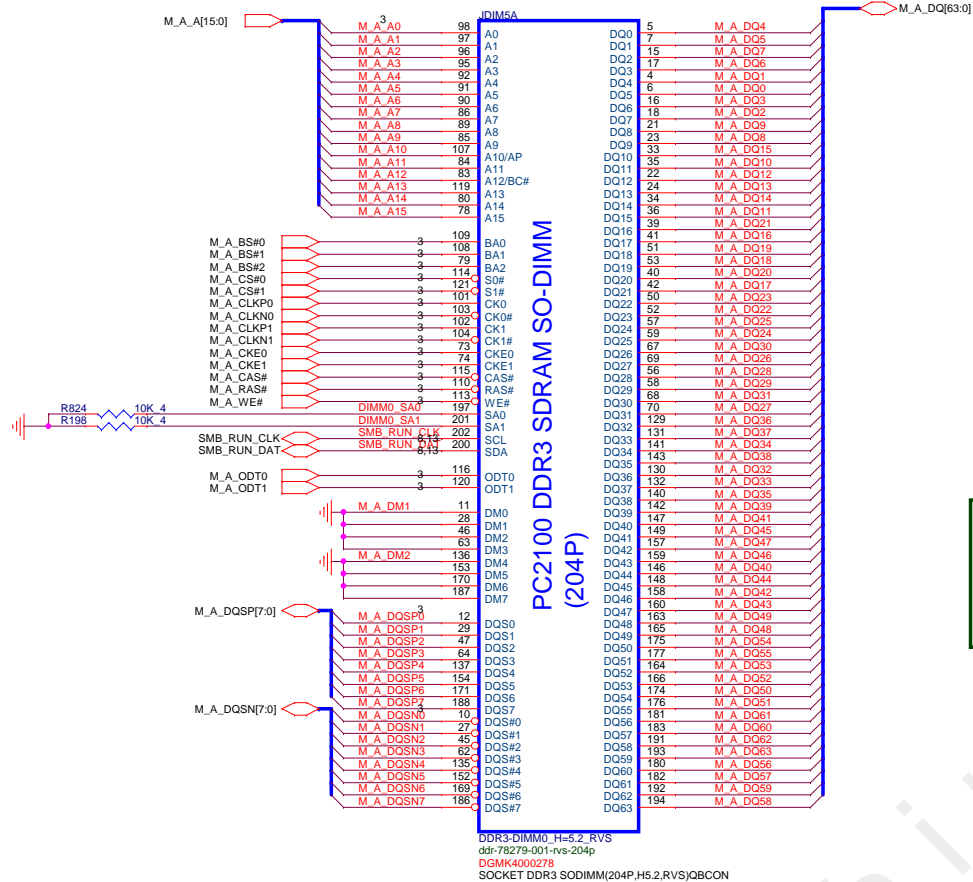
CPT_PPT_Rev_0p5

Cougar Point/Panther Point (GND)

HS	VSS[0]	AK38
AA17	VSS[1]	AK4
AA2	VSS[2]	VSS[80]
AA3	VSS[3]	VSS[81]
AA33	VSS[4]	VSS[82]
AA34	VSS[5]	VSS[83]
AB11	VSS[6]	VSS[84]
AB14	VSS[7]	VSS[85]
AB39	VSS[8]	VSS[86]
AB4	VSS[9]	VSS[87]
AB43	VSS[10]	VSS[88]
AB5	VSS[11]	VSS[89]
AB7	VSS[12]	VSS[90]
AC19	VSS[13]	VSS[91]
AC2	VSS[14]	VSS[92]
AC21	VSS[15]	VSS[93]
AC24	VSS[16]	VSS[94]
AC33	VSS[17]	VSS[95]
AC34	VSS[18]	VSS[96]
AC46	VSS[19]	VSS[97]
AD10	VSS[20]	VSS[98]
AD11	VSS[21]	VSS[99]
AD12	VSS[22]	VSS[100]
AD13	VSS[23]	VSS[101]
AD19	VSS[24]	VSS[102]
AD24	VSS[25]	VSS[103]
AD26	VSS[26]	VSS[104]
AD27	VSS[27]	VSS[105]
AD33	VSS[28]	VSS[106]
AD34	VSS[29]	VSS[107]
AD36	VSS[30]	VSS[108]
AD37	VSS[31]	VSS[109]
AD38	VSS[32]	VSS[110]
AD39	VSS[33]	VSS[111]
AD4	VSS[34]	VSS[112]
AD40	VSS[35]	VSS[113]
AD42	VSS[36]	VSS[114]
AD43	VSS[37]	VSS[115]
AD45	VSS[38]	VSS[116]
AD46	VSS[39]	VSS[117]
AD8	VSS[40]	VSS[118]
AE2	VSS[41]	VSS[119]
AE3	VSS[42]	VSS[120]
AF10	VSS[43]	VSS[121]
AF12	VSS[44]	VSS[122]
AD14	VSS[45]	VSS[123]
AD16	VSS[46]	VSS[124]
AF16	VSS[47]	VSS[125]
AF19	VSS[48]	VSS[126]
AF24	VSS[49]	VSS[127]
AF26	VSS[50]	VSS[128]
AF27	VSS[51]	VSS[129]
AF29	VSS[52]	VSS[130]
AF31	VSS[53]	VSS[131]
AF38	VSS[54]	VSS[132]
W2	VSS[55]	VSS[133]
AF4	VSS[56]	VSS[134]
AF42	VSS[57]	VSS[135]
AF46	VSS[58]	VSS[136]
AF5	VSS[59]	VSS[137]
AF7	VSS[60]	VSS[138]
AF8	VSS[61]	VSS[139]
AG19	VSS[62]	VSS[140]
AG2	VSS[63]	VSS[141]
AG31	VSS[64]	VSS[142]
AG46	VSS[65]	VSS[143]
AH11	VSS[66]	VSS[144]
AH3	VSS[67]	VSS[145]
AH36	VSS[68]	VSS[146]
AH38	VSS[69]	VSS[147]
AH40	VSS[70]	VSS[148]
AH42	VSS[71]	VSS[149]
AH46	VSS[72]	VSS[150]
AH7	VSS[73]	VSS[151]
AJ19	VSS[74]	VSS[152]
AJ21	VSS[75]	VSS[153]
AJ24	VSS[76]	VSS[154]
AJ33	VSS[77]	VSS[155]
AJ34	VSS[78]	VSS[156]
AK12	VSS[79]	VSS[157]
AK3		VSS[158]

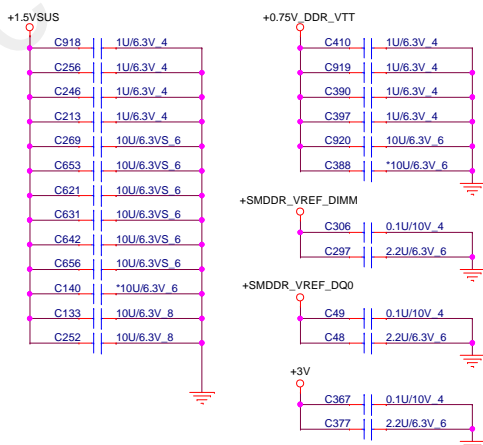
CPT_PPT_Rev_0p5



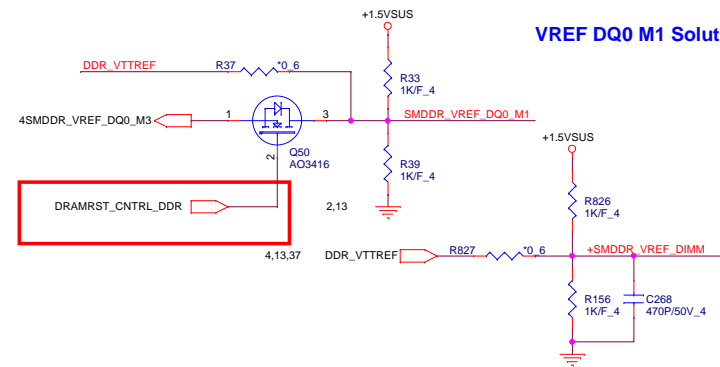


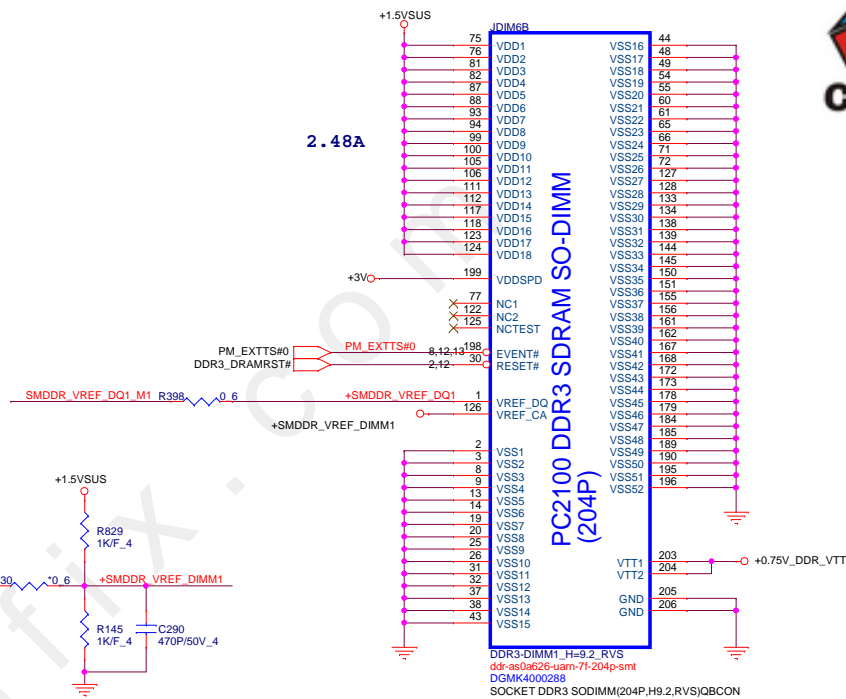
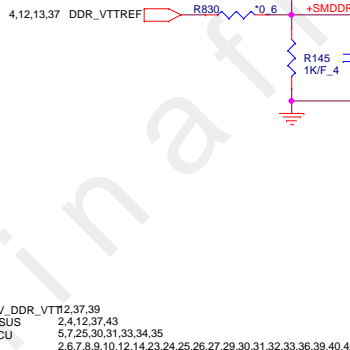
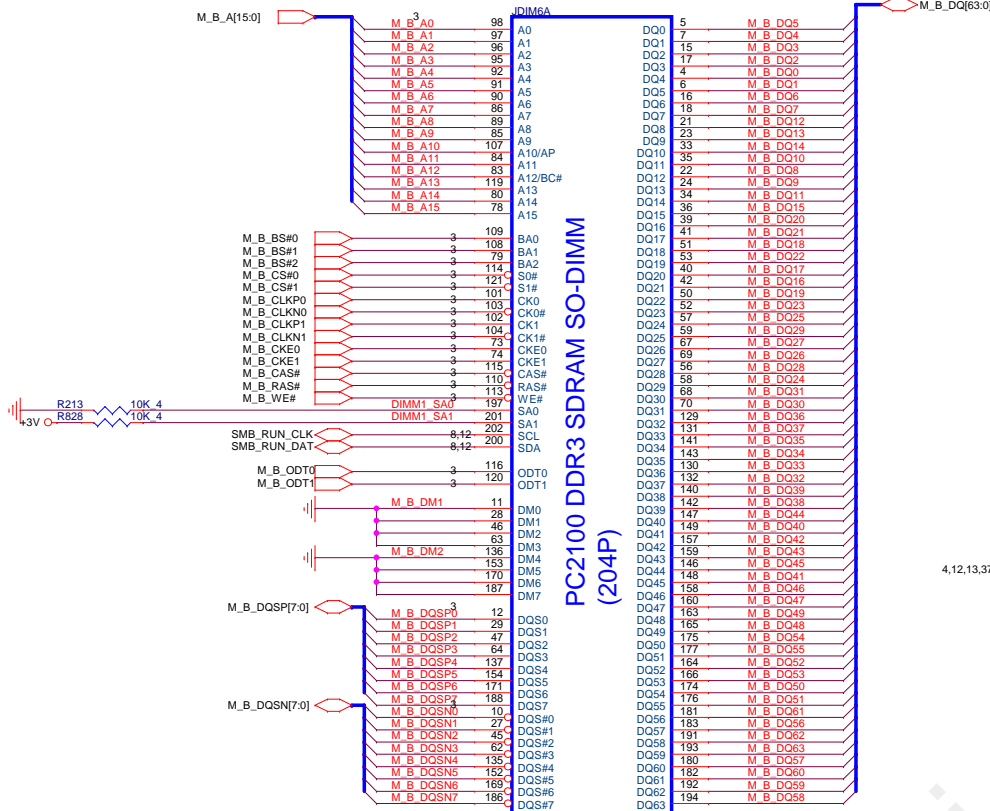
+1.5V	4,10,27,33
+0.75V_DDR_VTT#	3,37,39
+1.5VSUS	2,4,13,37,43
+3VPCU	5,7,25,30,31,33,34,35
+3V	2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

Place these Caps near So-Dimm0.

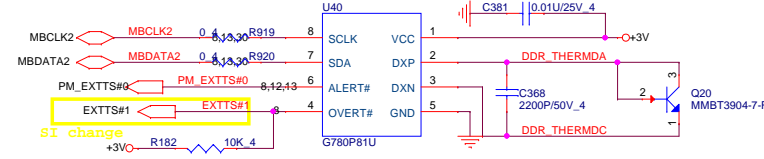


VREF DQ0 M1 Solution

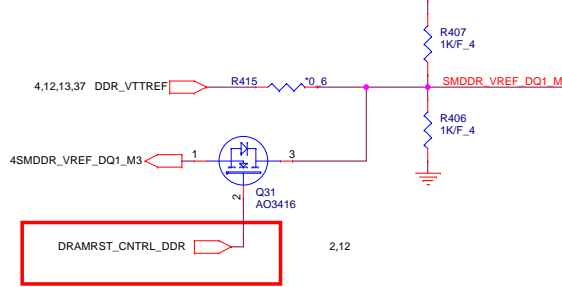




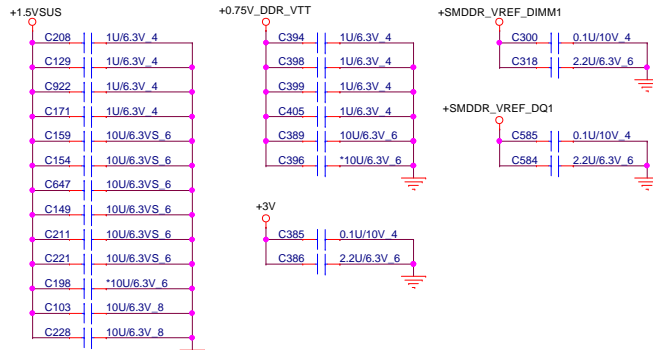
DDR3 Thermal Sensor



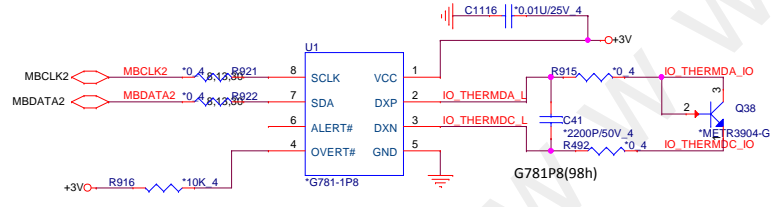
VREF DQ1 M1 Solution

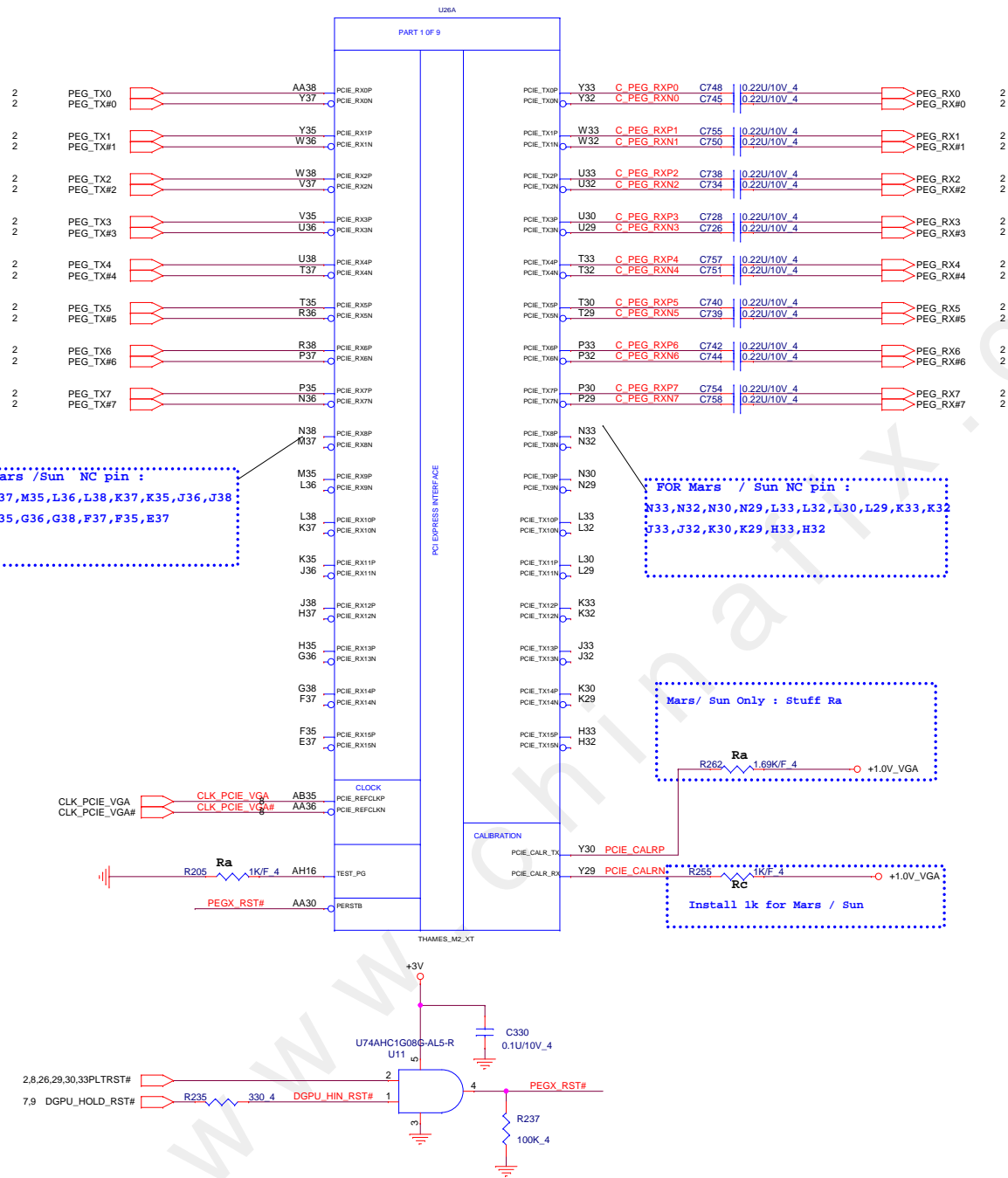


Place these Caps near So-Dimm1.



Local Thermal Sensor





2,6,7,8,9,10,12,13,23,24,25,26,27,29,30,31,32,33,36,39,40,42
16,18,19,43 +1.0V_VGA

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

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For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

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For Mars / Sun : AR1/AR6/AR3/AR8/AUS; NC pin

MLPS Implementation

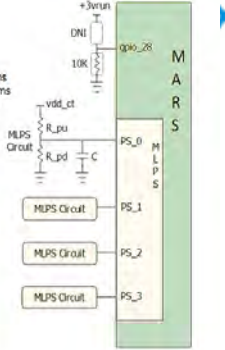
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

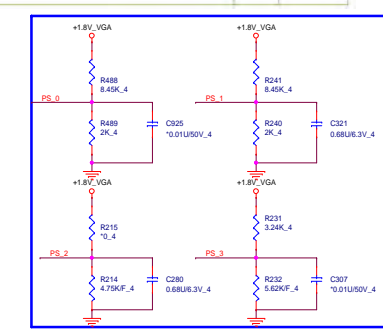
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romddg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romddg[2:0] define memory aperture size. If bios_rom_en = 1, romddg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen0_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ# supported	x	gpio_8
PS_1[3]	n/a	Reserved	x	genk_clk
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved	n/a	n/a
PS_2[2]	n/a	Reserved	n/a	n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_ds	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved	n/a	n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_ep[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_ep[1]			
PS_3[0]	aud_port_ep[0]			

PS0 => 11001
PS1 => 00001
PS2 => 00000
PS3 => 11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K



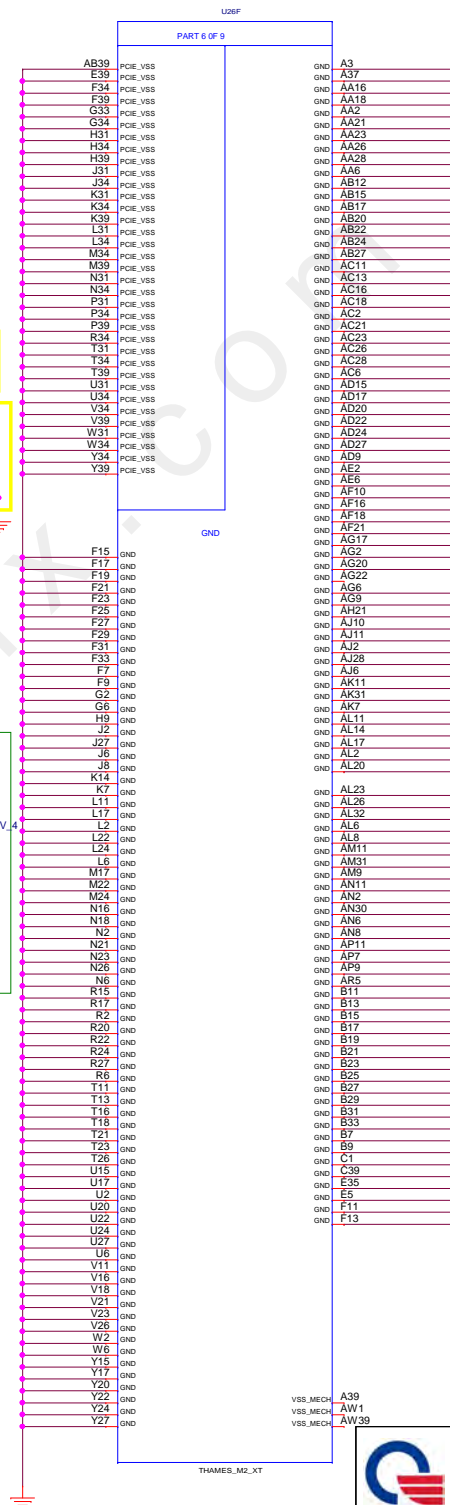
PS3 BIT3==>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	AKD5P0WTW08 IC SDRAM/96P/H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M10HA-093GE	AKD5P23T101 IC SDRAM/96P/MT41J256M10HA-093GE	2G
010	2	Samsung	K4W4G1646B-HC1A	AKD5P2D1T03 IC SDRAM/96P/K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FR-11C	AKD5M2D1W03 IC SDRAM/96P/H5TC2G63FR-11C	1G
100	4	Micron	MT41J128M161T-093GE	AKD5M2D1W03 IC SDRAM/96P/MT41J128M161T-093GE	1G
101	5	Samsung	K4W2G1646E-BC1A	AKD5M2D1W03 IC SDRAM/96P/K4W2G1646E-BC1A	1G



[illegible]

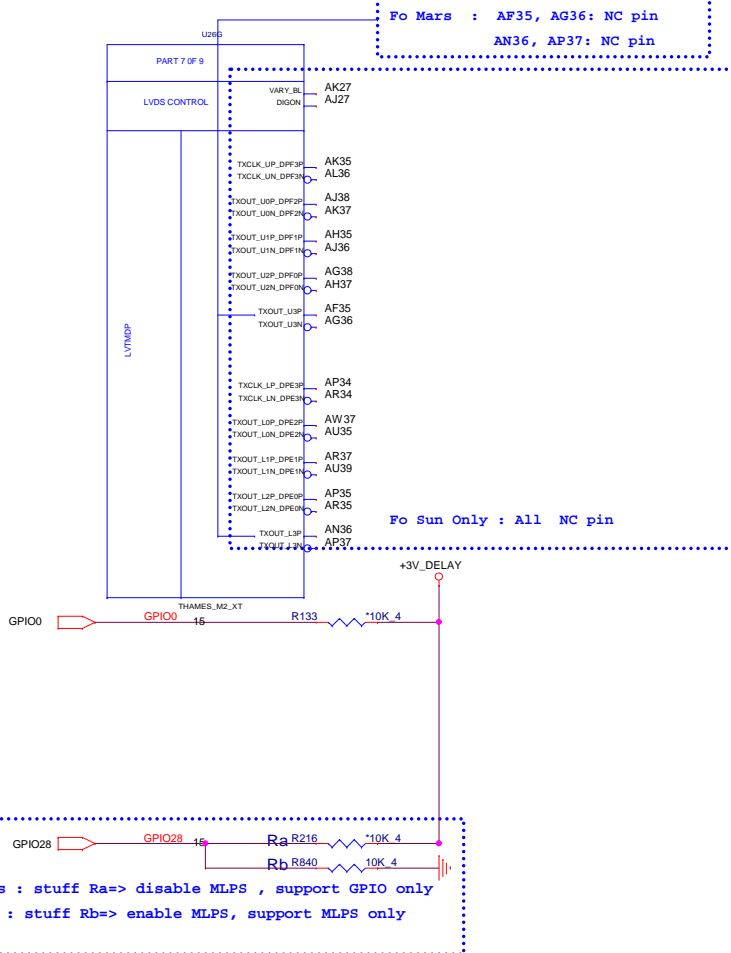
Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short



AG22 is nc pin





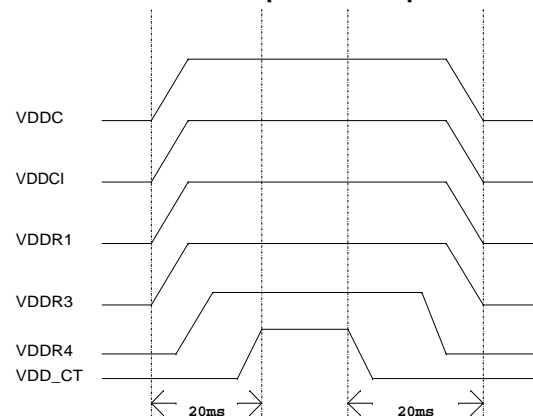
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

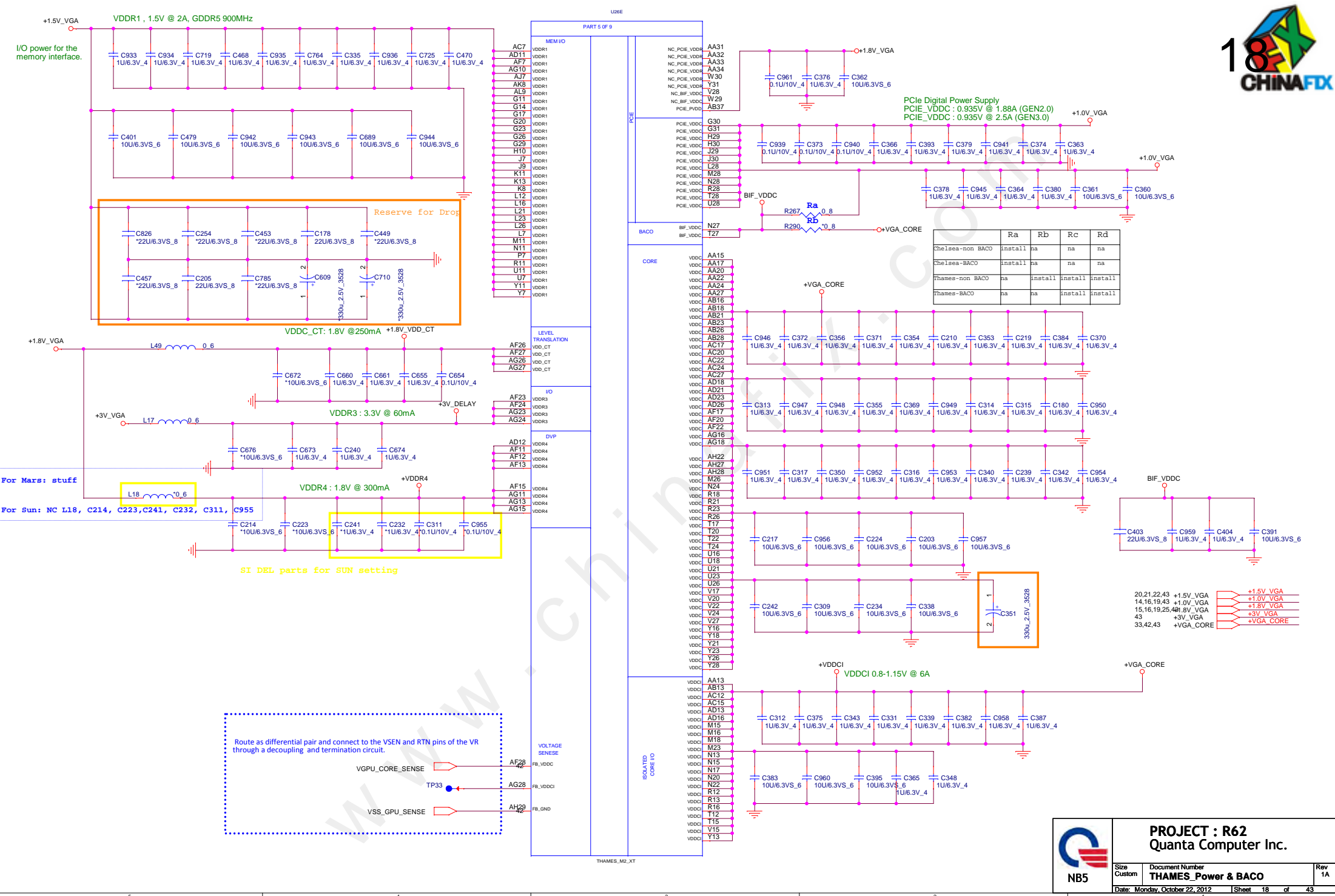
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

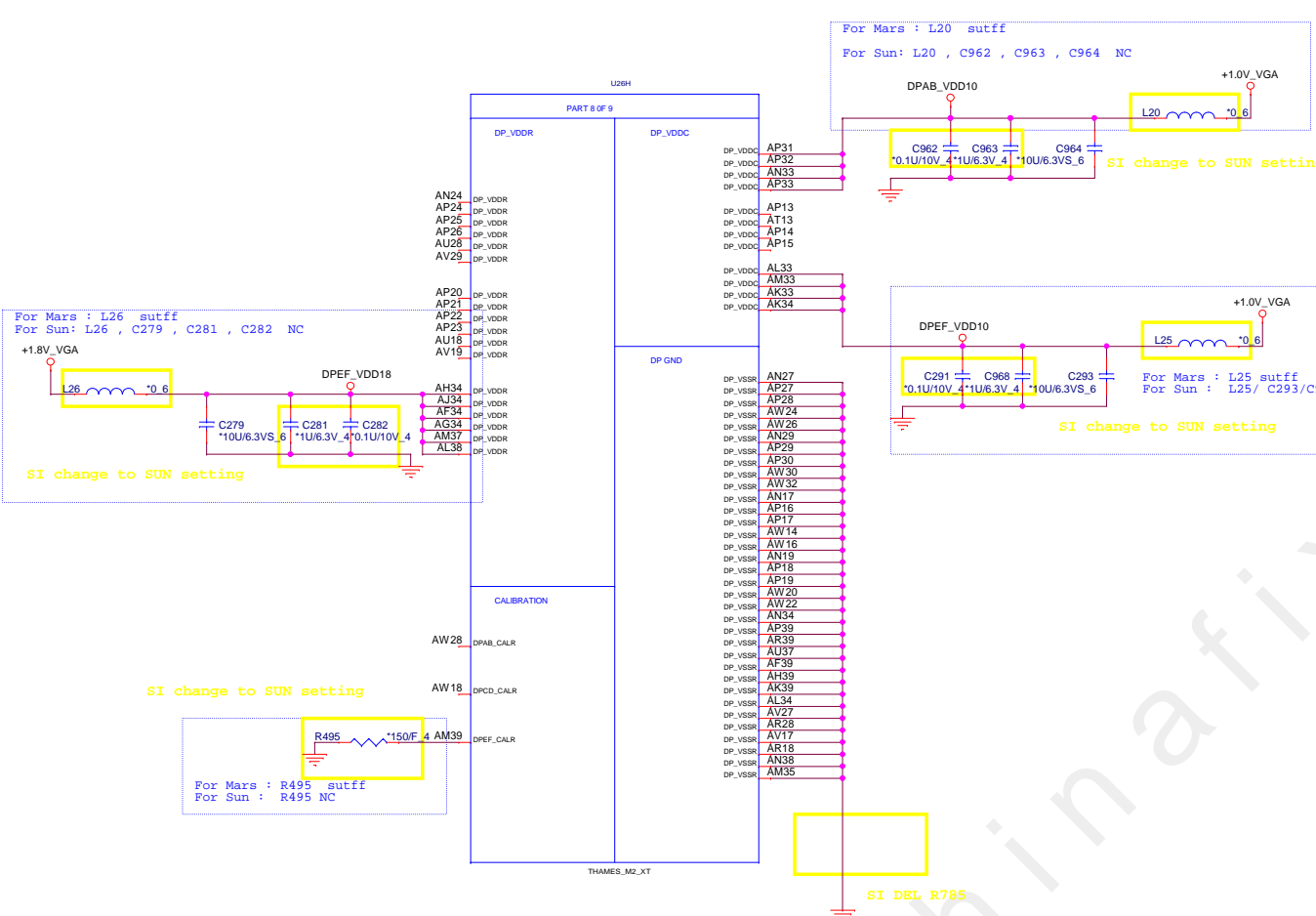
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P20 (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P40 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYN	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

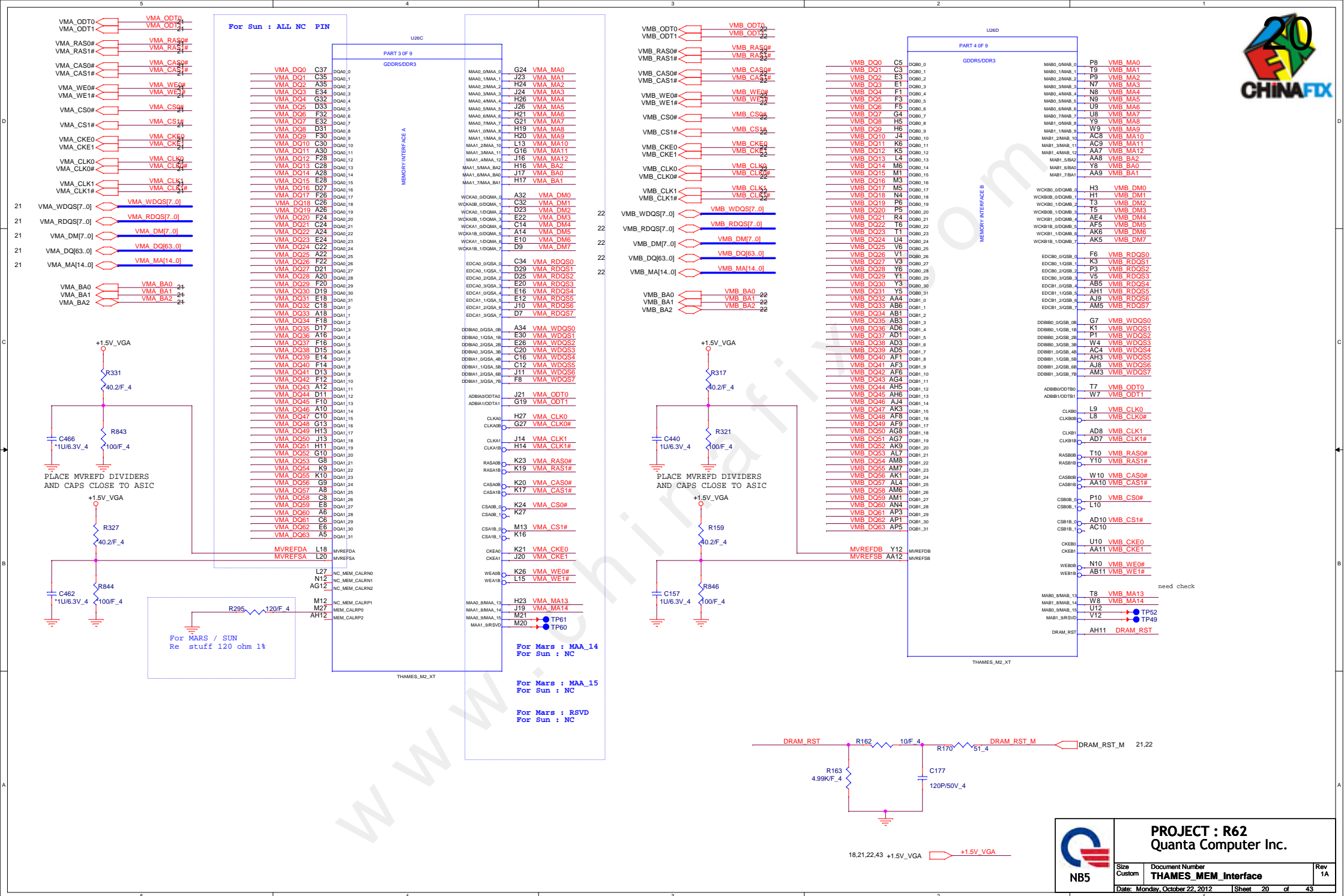
Power Up/Down Sequence



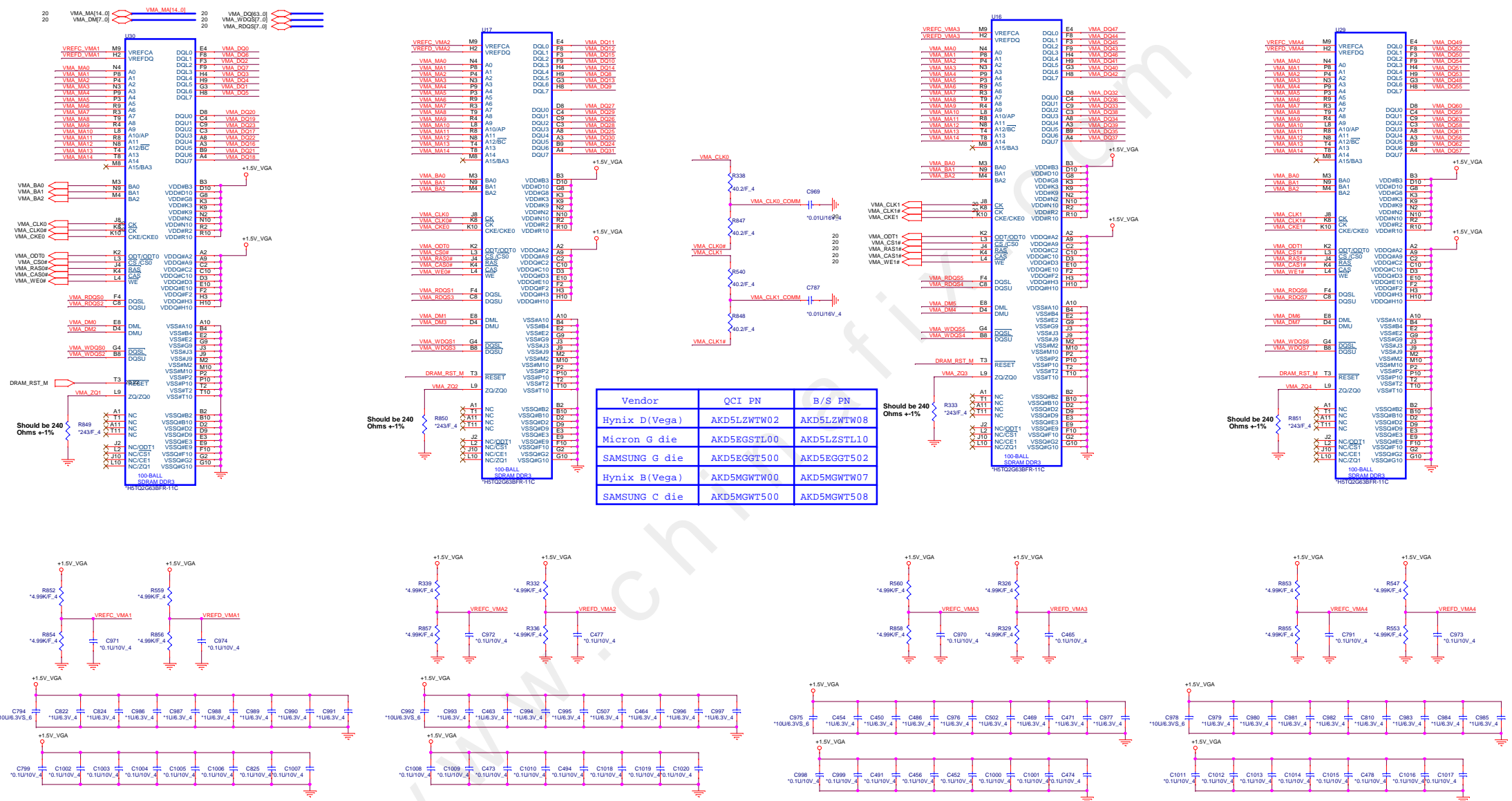
PROJECT : R62 Quanta Computer Inc.		Rev 1A
Size Custom	Document Number THAMES_LVDS / STRAP	
Date: Monday, October 22, 2012	Sheet 17 of 43	





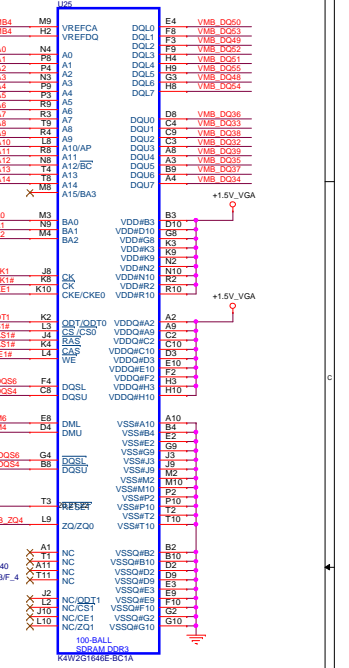
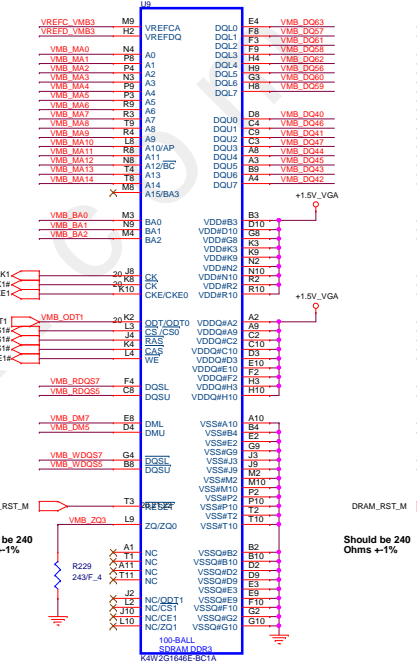
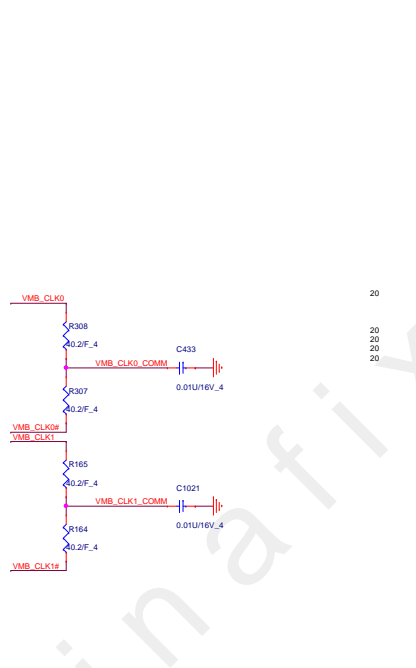
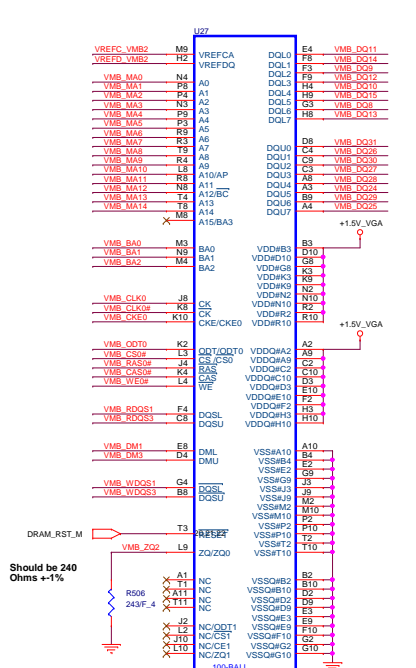
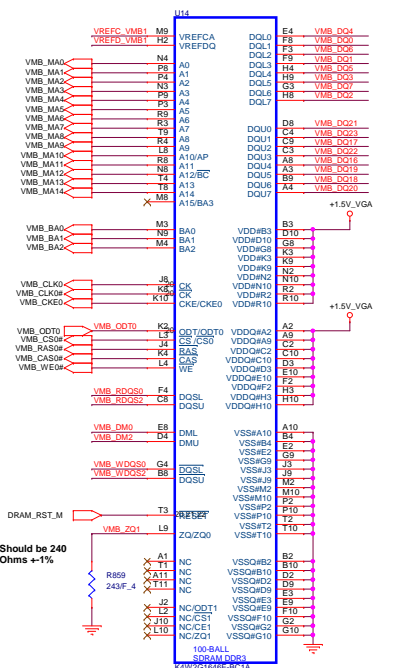


CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

20.22 VMB_MA[14:0] VMB_MA[14:0]
20 VMB_DM[7:0] VMB_DM[7:0]

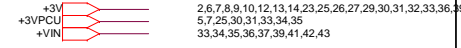
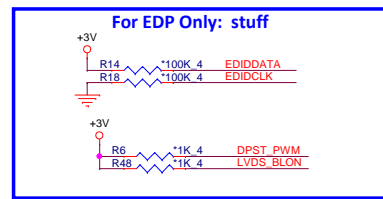
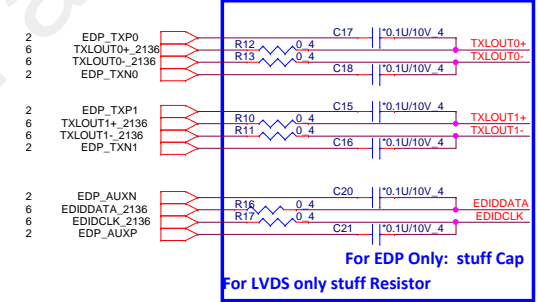
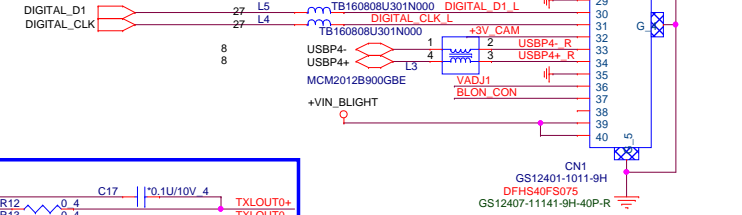
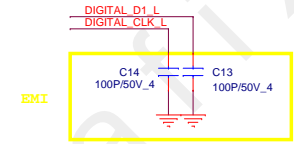
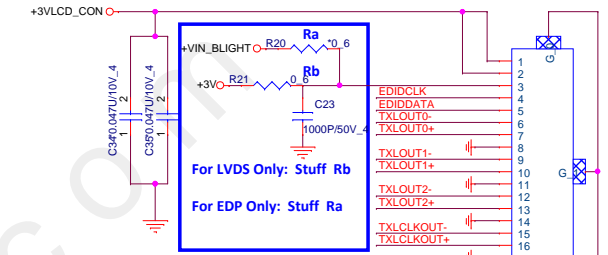
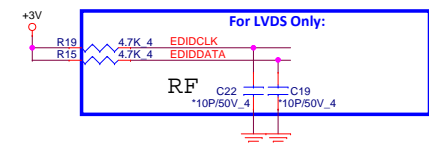
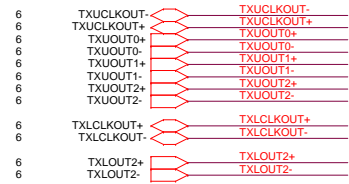
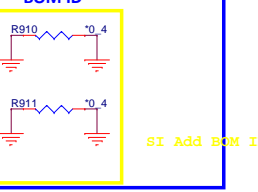
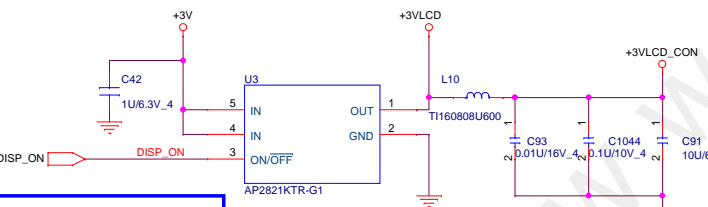
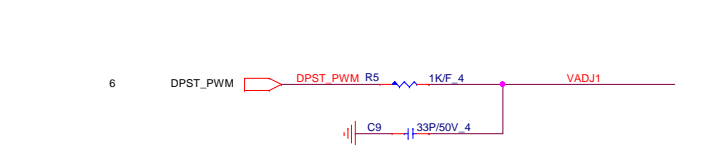
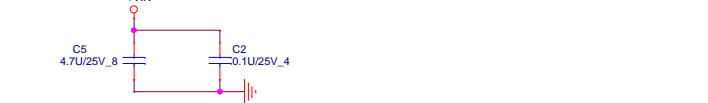
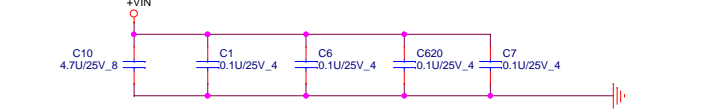
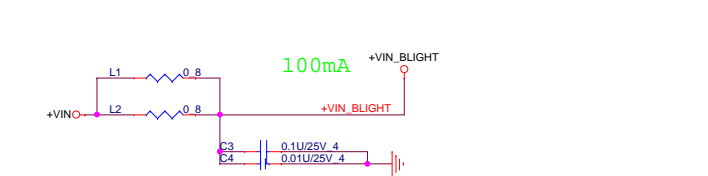
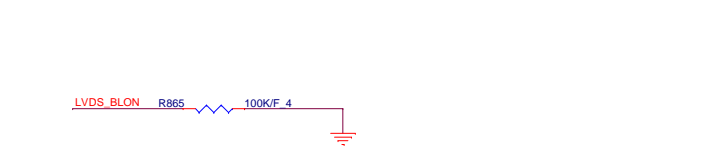


HOLE



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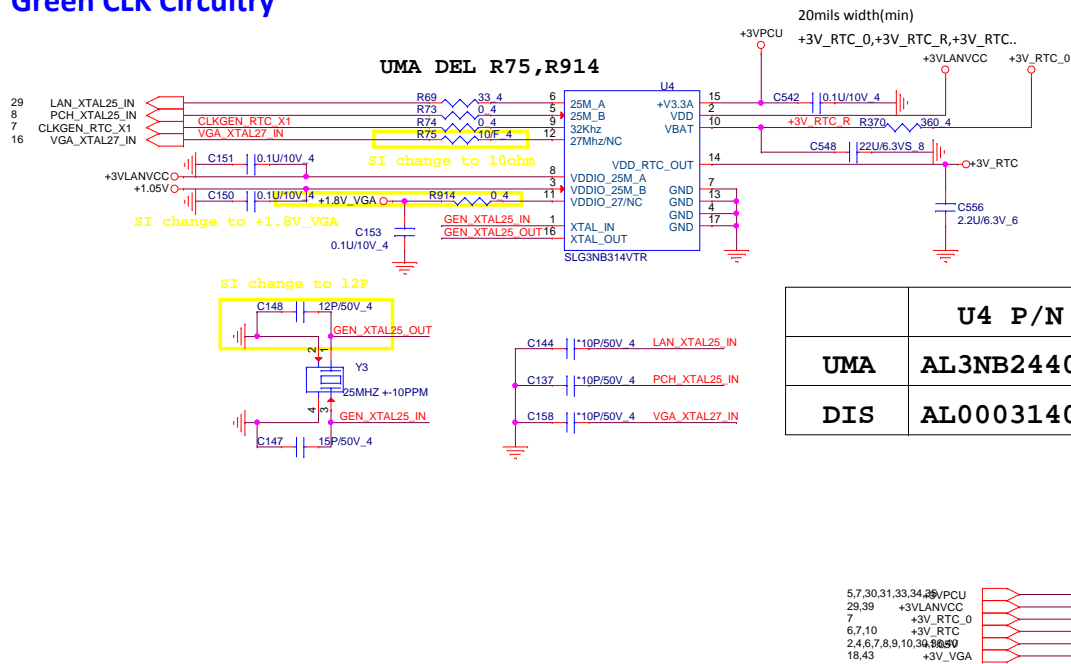
LID Switch



2,6,7,8,9,10,12,13,14,23,25,26,27,29,30,31,32,33,36,35,5,7,25,30,31,33,34,35,33,34,35,36,37,39,41,42,43

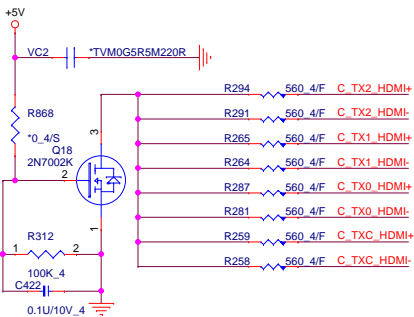
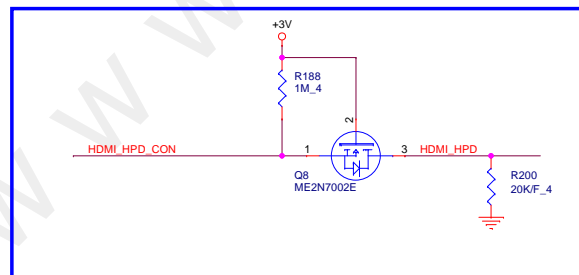
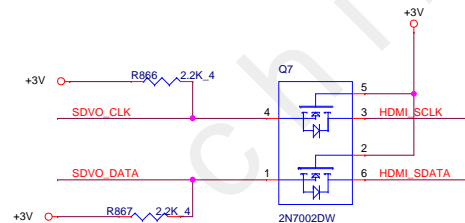
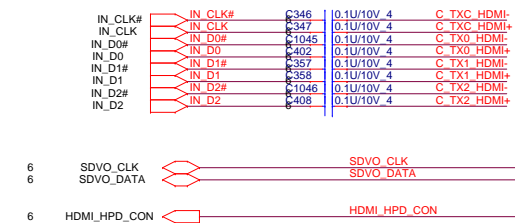


Green CLK Circuitry

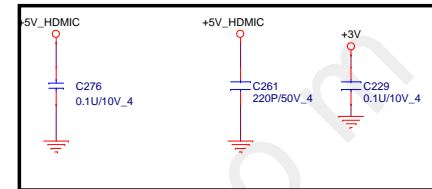


close to HDMI conn

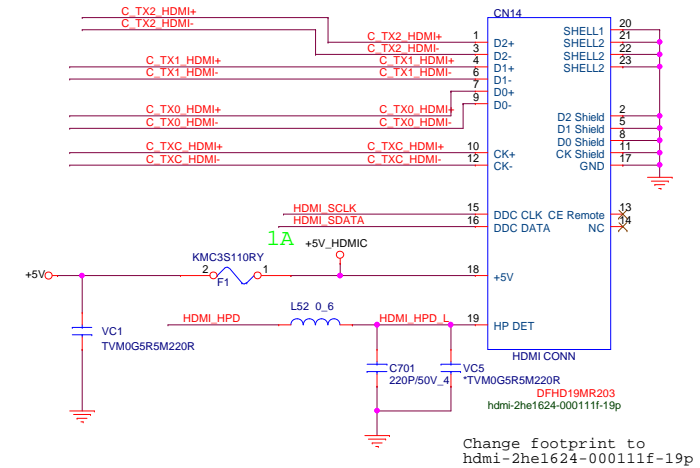
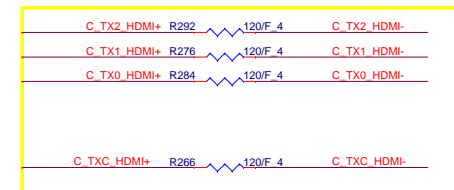
Close to HDMI Connector



EMI request



EMI request



Change footprint to hdmi-2he1624-000111f-19p

8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4/S CLK_PCIE_REQ2#_R

SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

Close to chip pin

8 CLK_PCIE_CARDP
8 CLK_PCIE_CARDN
8 PCIE_RXP3_CARD
8 PCIE_RXN3_CARD

PCIE_TXP3_CARD
PCIE_TXN3_CARD
C598 0.1U/10V_4
C597 0.1U/10V_4

Please add 9 GND VIAS
connection with thermal PAD

Close to chip pin

SP6 SD D2_R R871 0.4 SD D2
SP5 SD D3_R R443 0.4 SD D3
SP4 SD CMD_R R444 0.4 SD CMD
SP3 DV33_18
SP2 SD CLK_R R441 22.4 SD CLK
SD D0_R R448 0.4 SD D0

Reserve for EMI

SD D0	C1069	*5.6P/16V_4
SD D1	C612	*5.6P/16V_4
SD D2	C611	*5.6P/16V_4
SD D3	C1068	*5.6P/16V_4

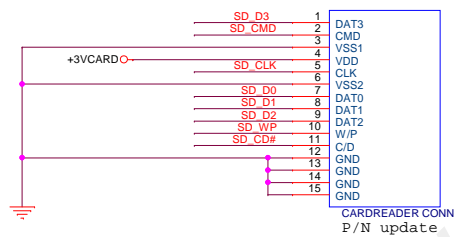
Close to U38

R435 need colse to Chip

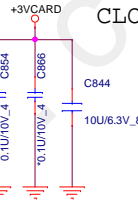
SD / MMC

CARD READER

CN8



CLOSE CONN

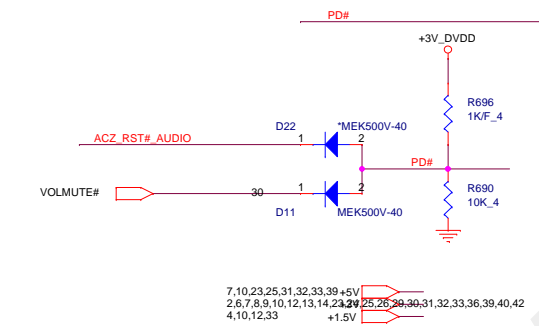
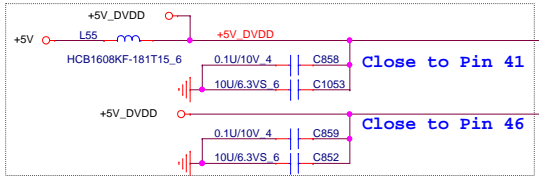
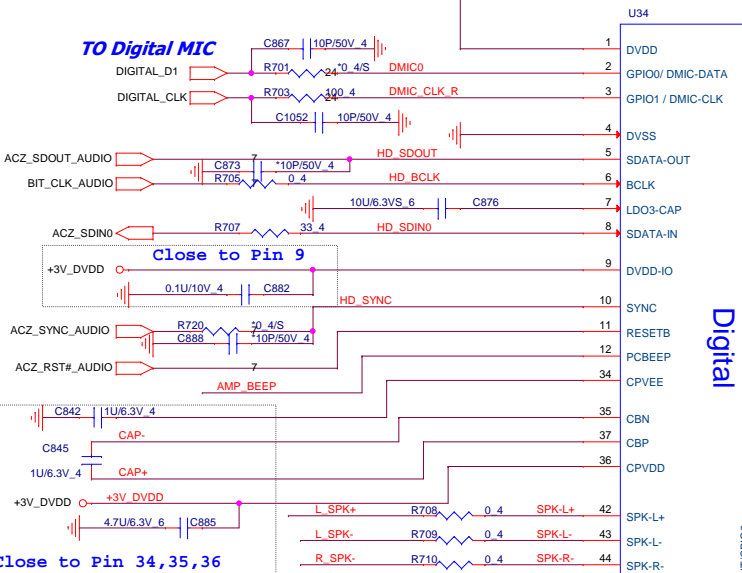
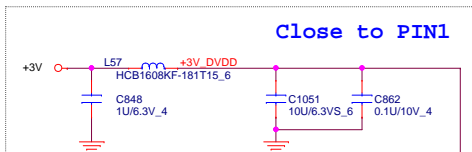


Reserve for EMI

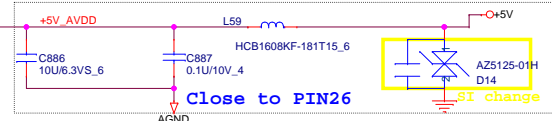
SD D0	C1049	*5.6P/16V_4
SD D1	C886	*5.6P/16V_4
SD D2	C610	*5.6P/16V_4
SD D3	C1050	*5.6P/16V_4
SD CLK	C1100	*5.6P/16V_4

Close to CN8

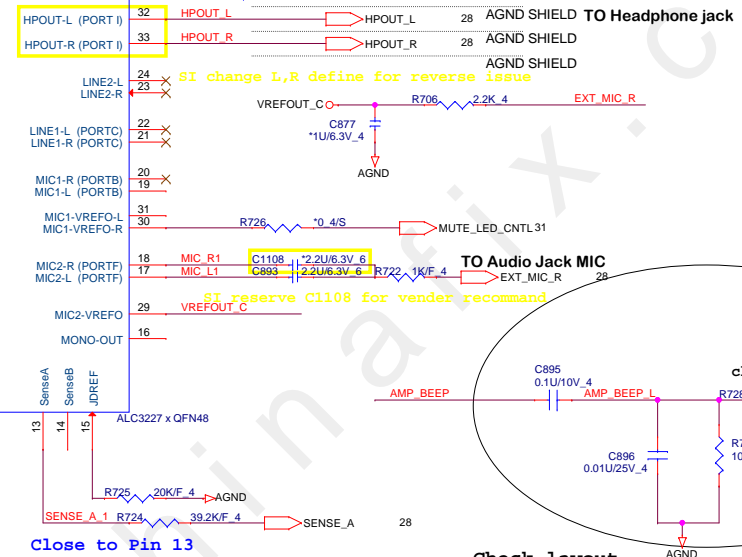
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42



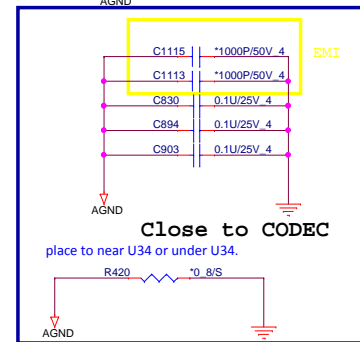
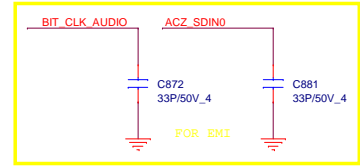
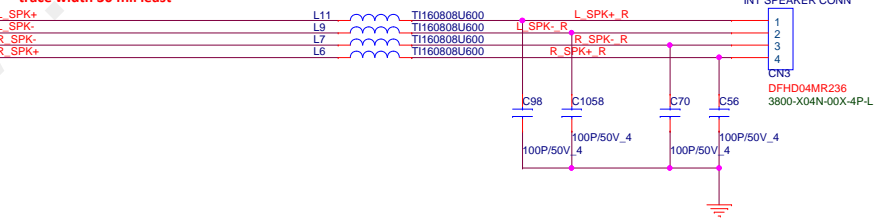
>40mils trace



Analog

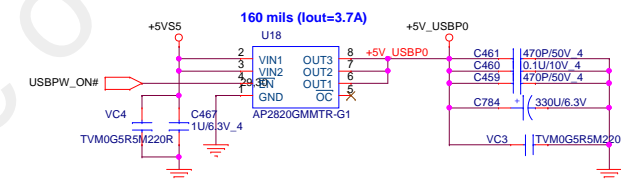


Close to CODEC
Speaker 4 ohm: 40mils

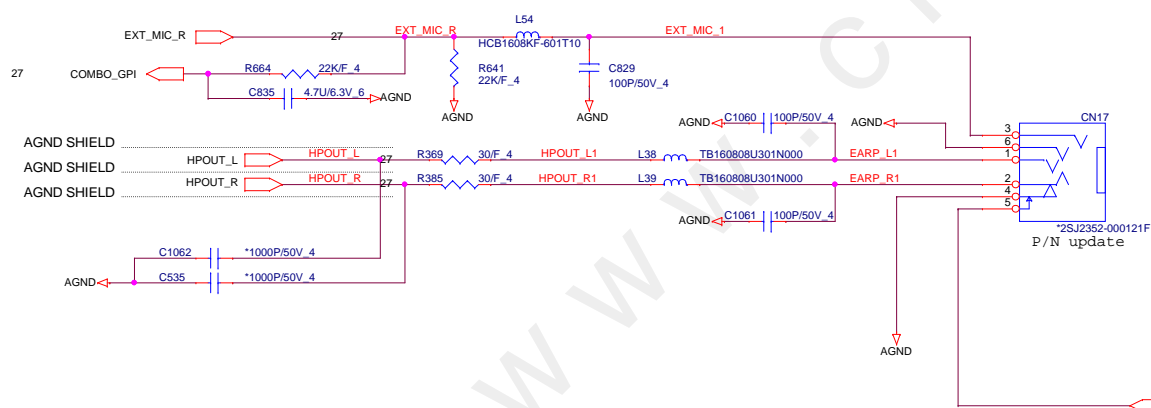


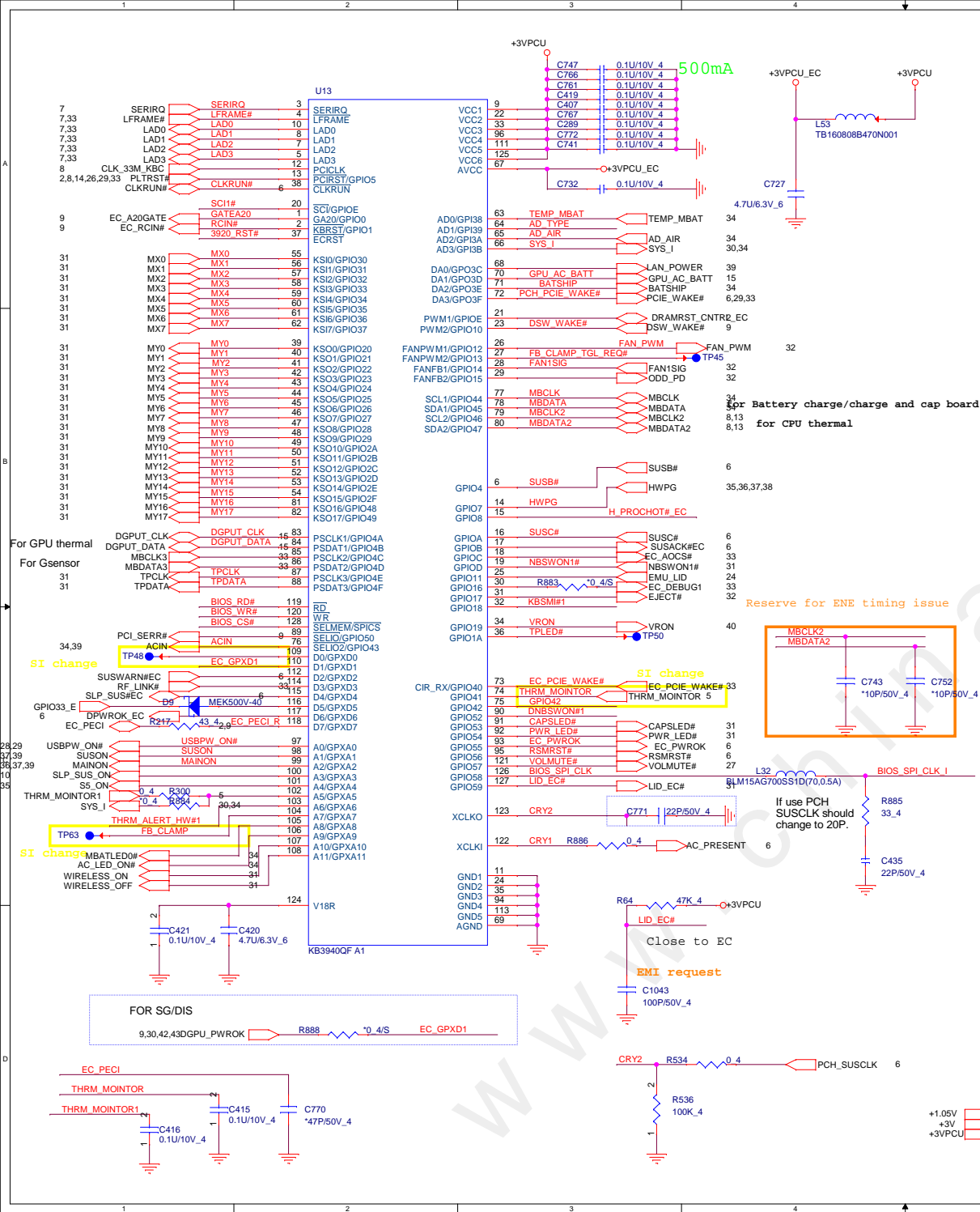


USB3.0 X 2/USB2.0 COMBO

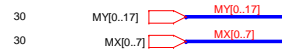


COMBO JACK

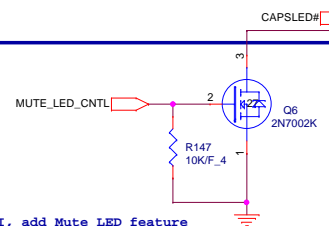
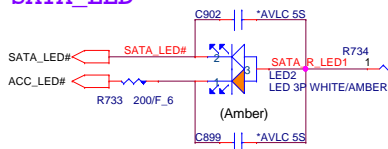




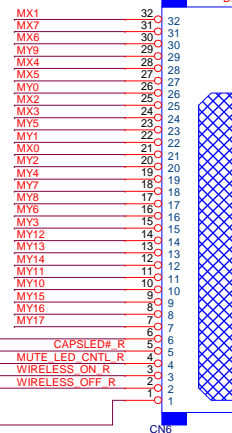
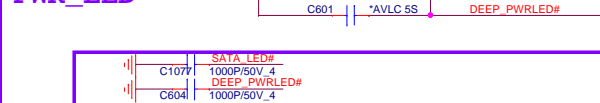
KEYBOARD Con.



SATA_LED

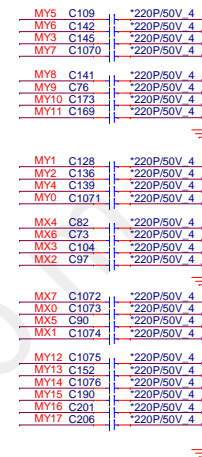
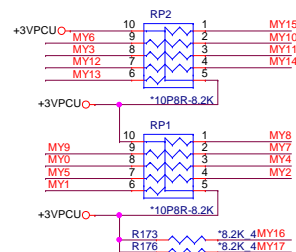


PWR_LED

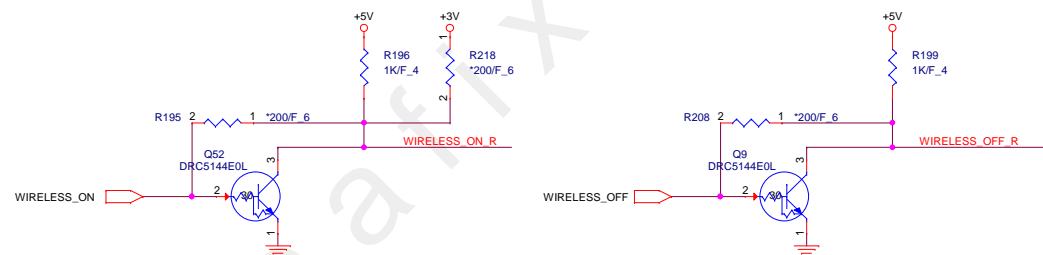


P/N update

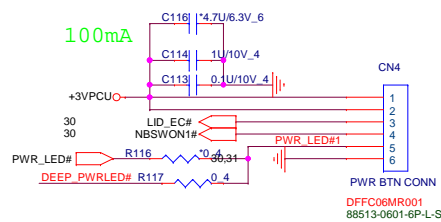
KEYBOARD PULL-UP



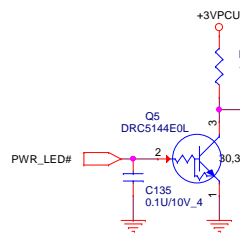
EC KB3930 has included K/B pull-up resistor and function



POWER BOTTON CONNECT

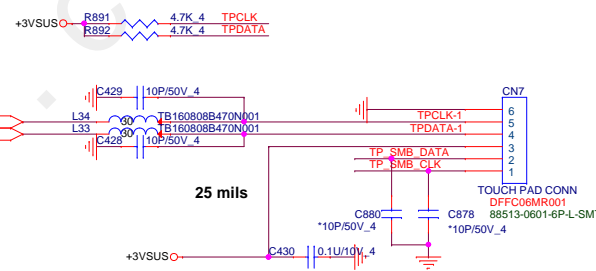


1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

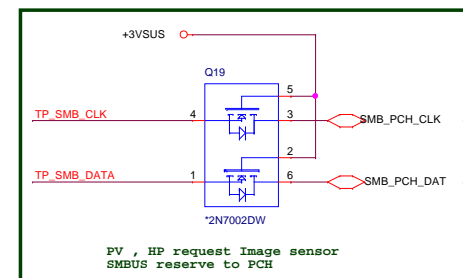


TOUCH PAD Con.

change to +3VSUS
close conn



Change footprint to 88513-0601-6P-L-SMT



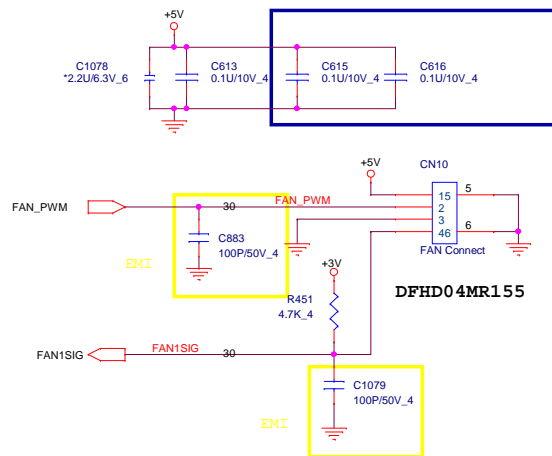
FV , HP request Image sensor
SMBUS reserve to PCH



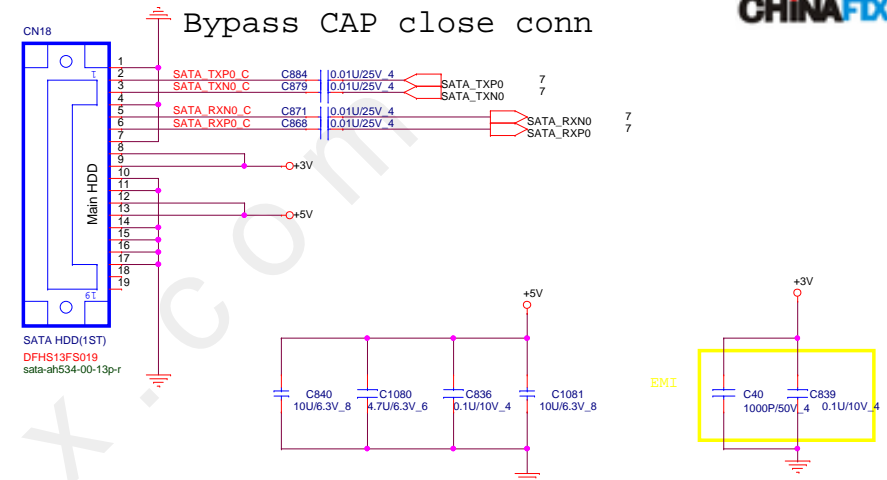
PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A
Date: Monday, October 22, 2012	Sheet 31 of 43	

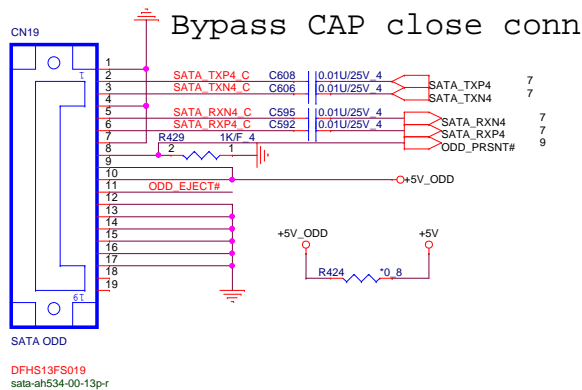
CPU FAN



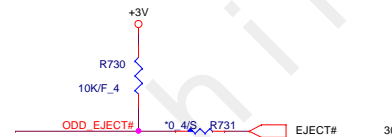
SATA HDD CONNECTOR



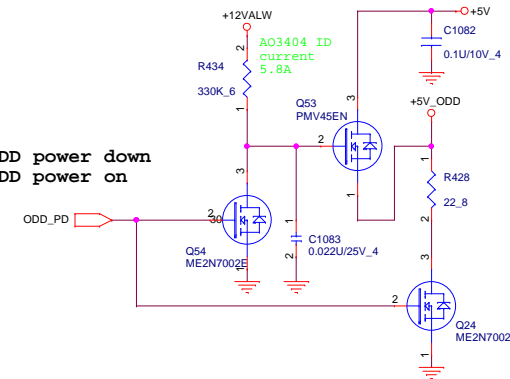
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on

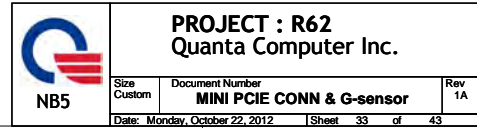


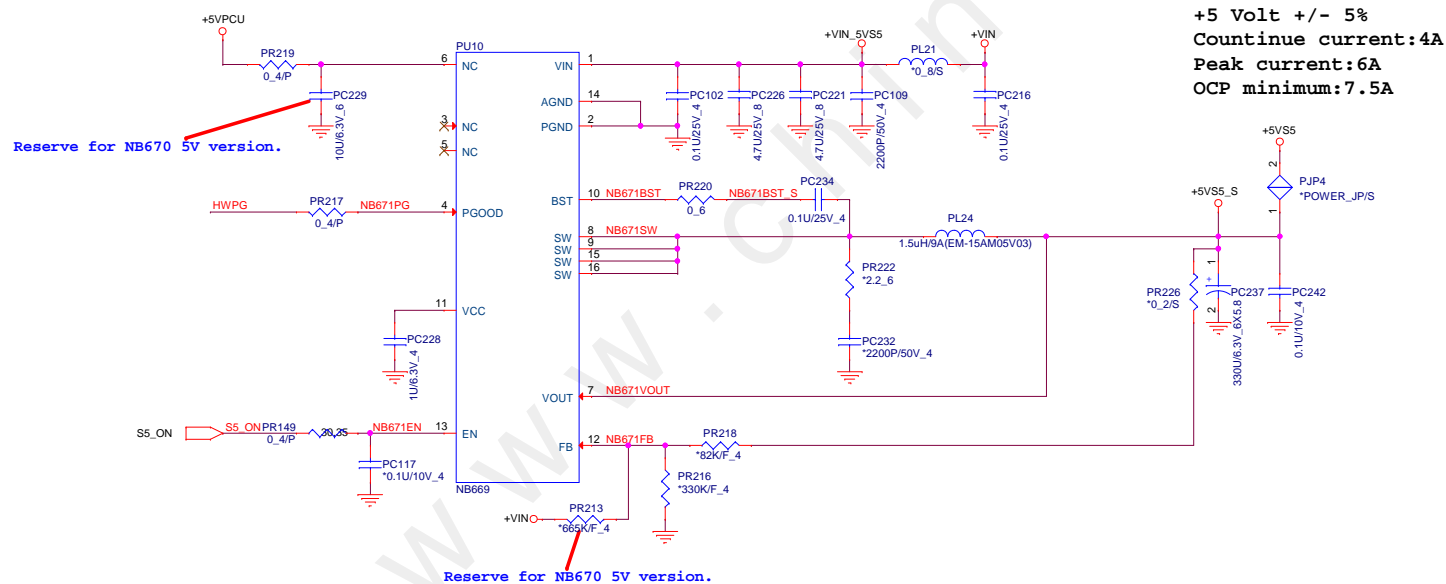
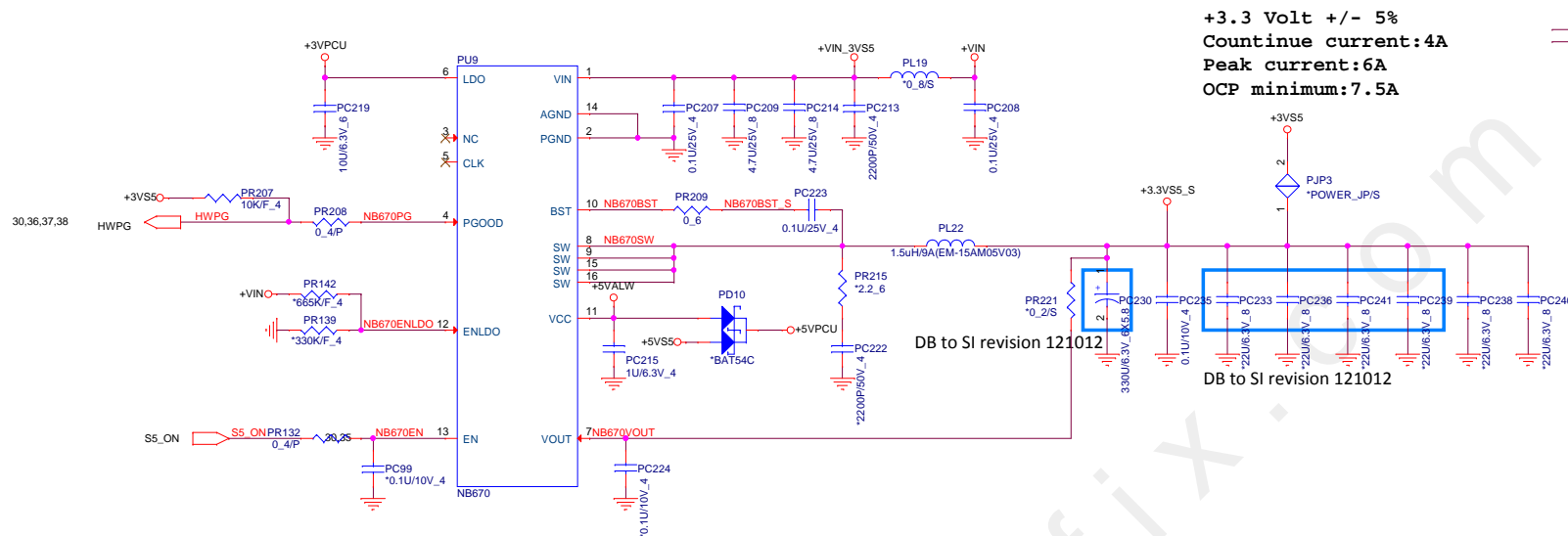
+3V
+3VPCU
+5V
+12VALW

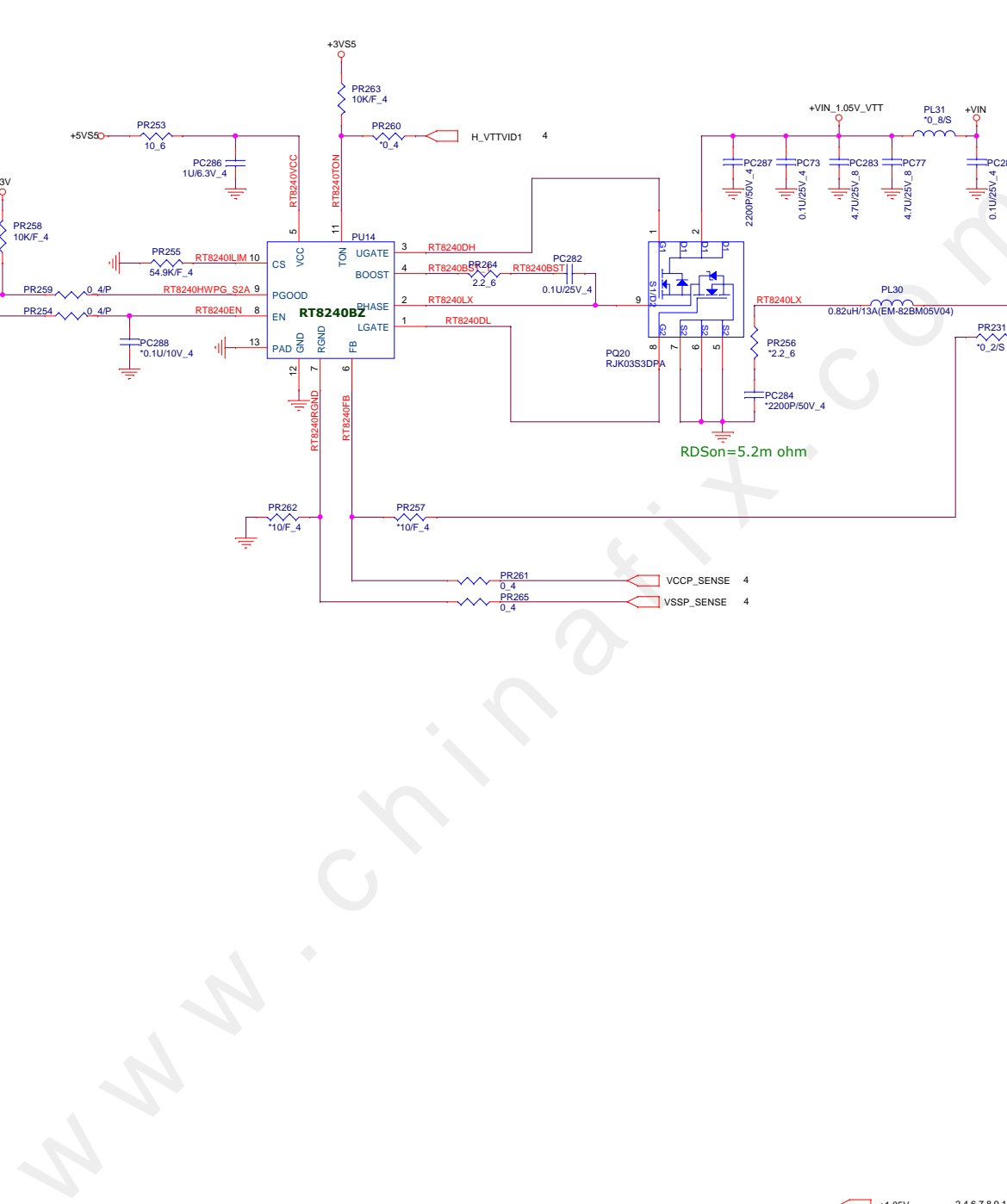
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
5,7,25,30,31,33,34,35
7,10,23,25,27,31,33,39
34,39,43



D




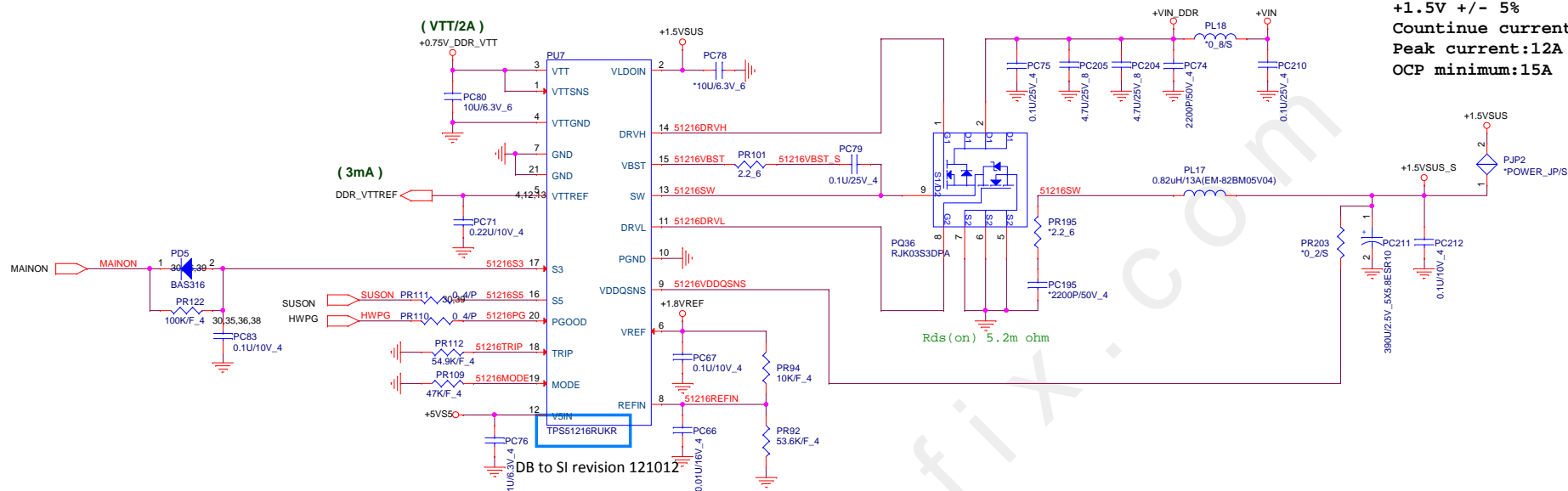




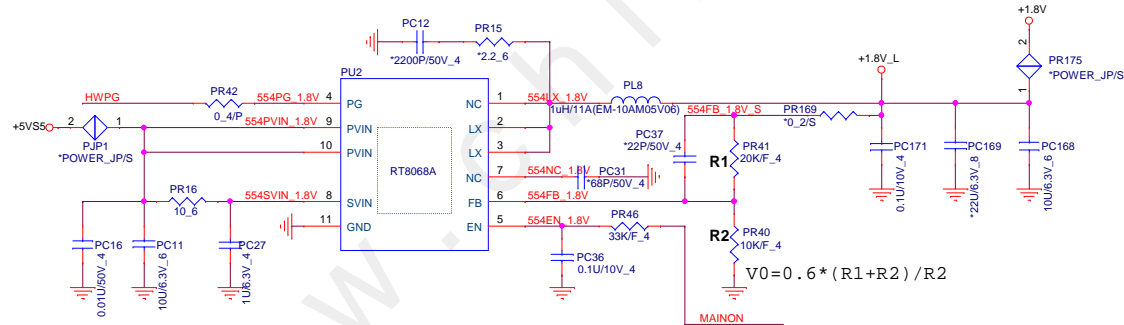
600 mils

PDSe₀-5 2m ohm

 NB5	PROJECT : R62 Quanta Computer Inc.		
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	Date: Monday, October 22, 2012	Sheet 36 of 43	



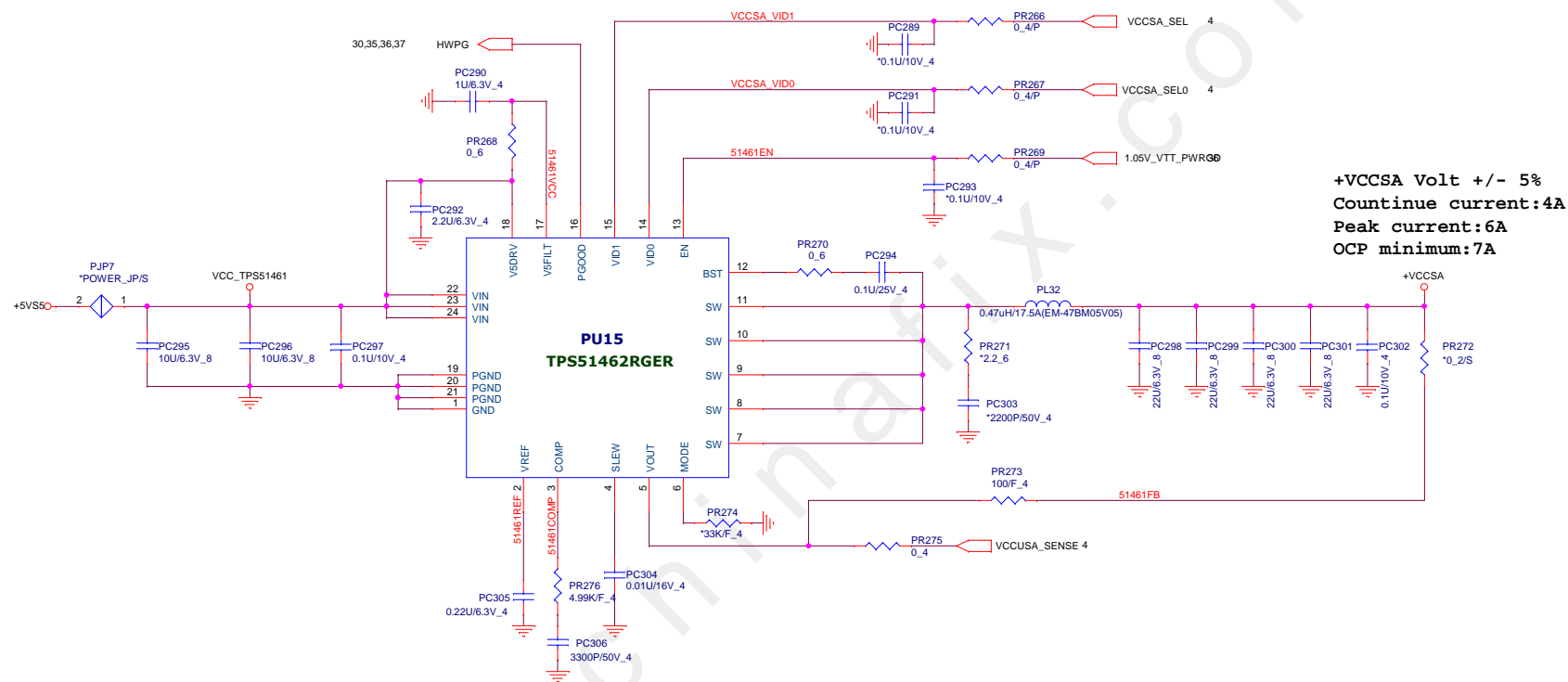
1.8V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A

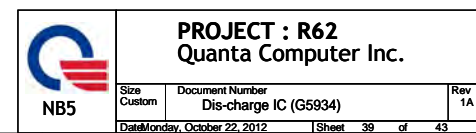


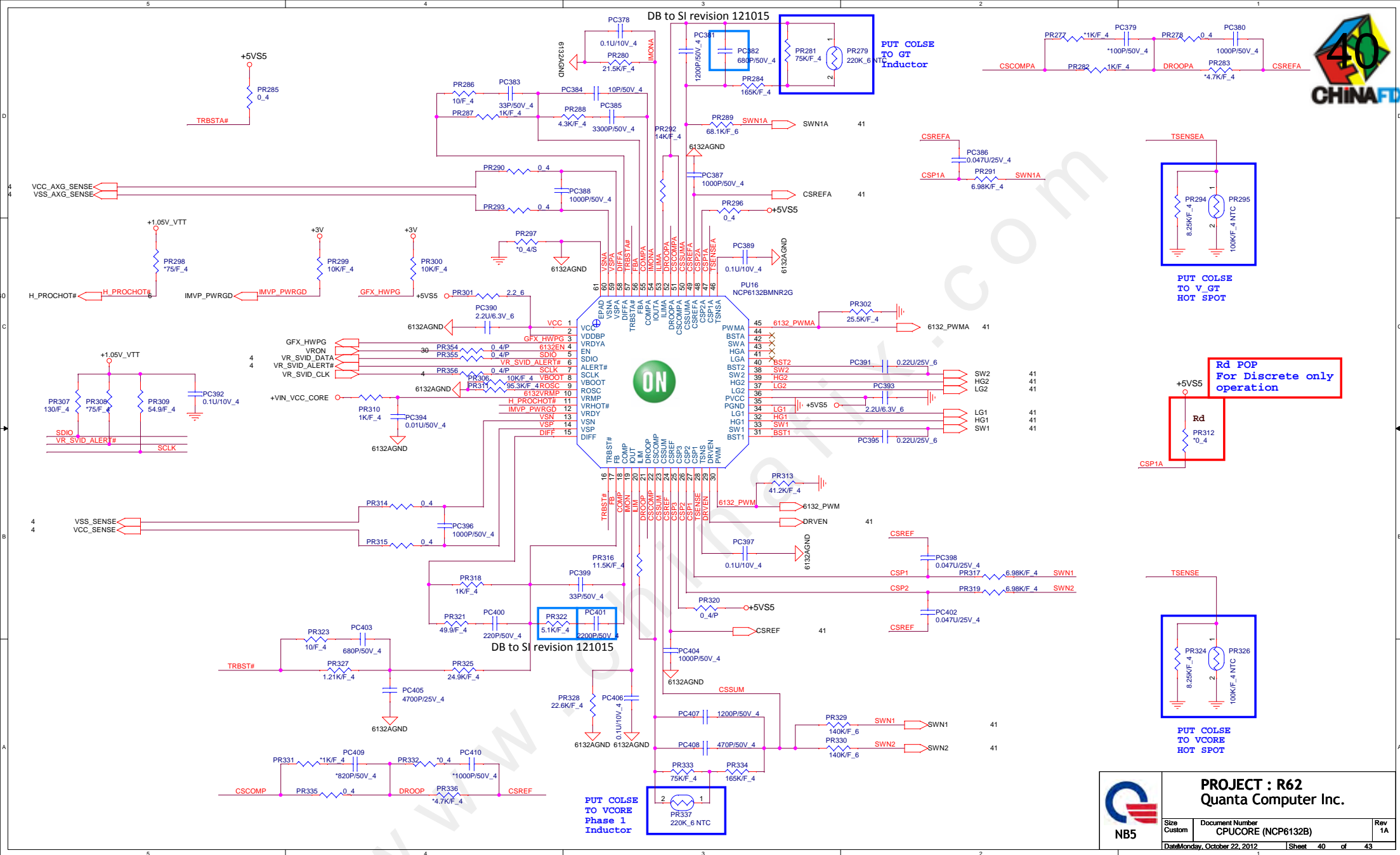
TPSS1462RGER/AL051462000

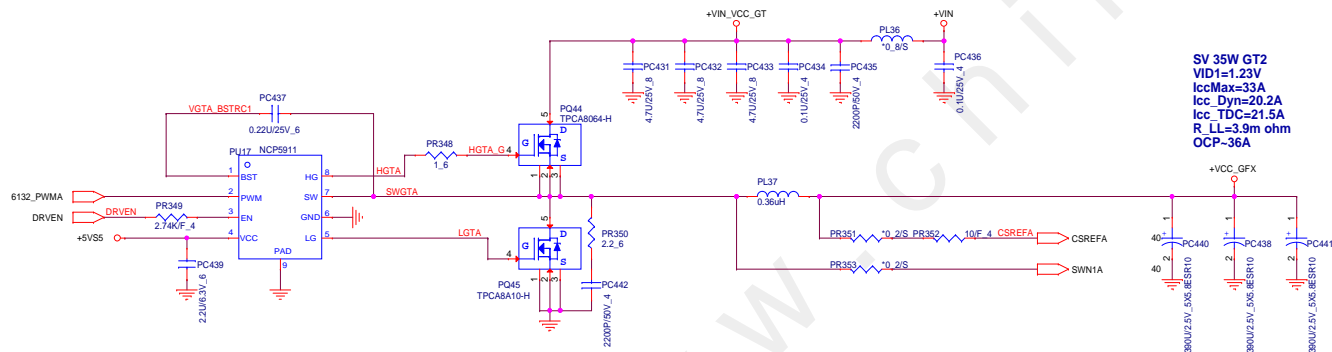
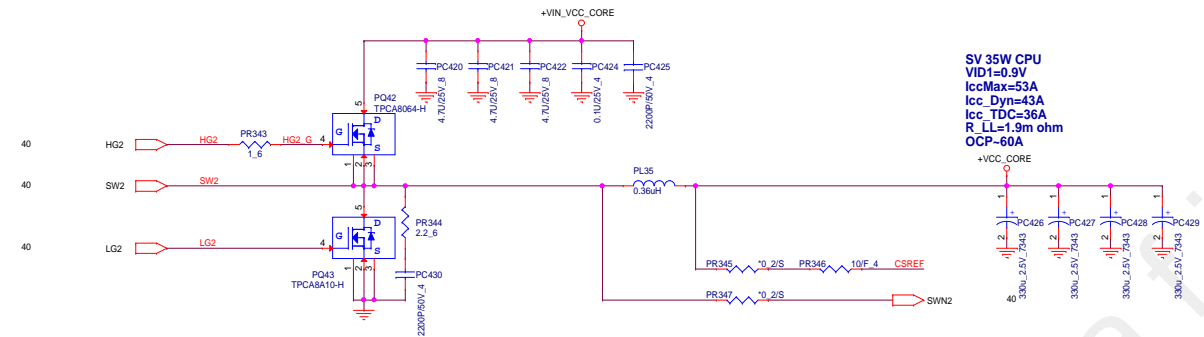
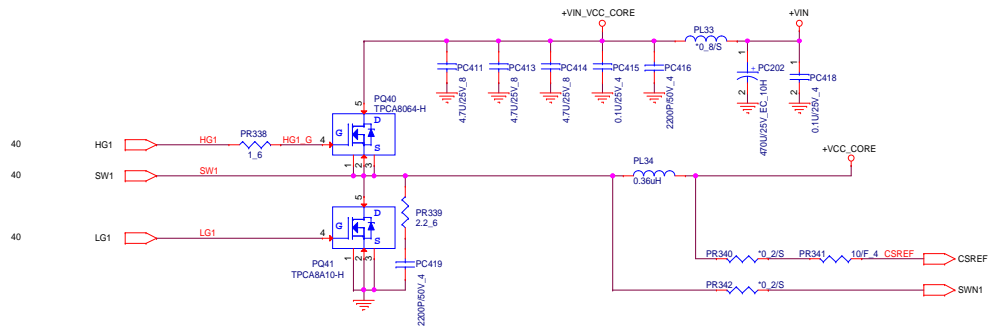
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



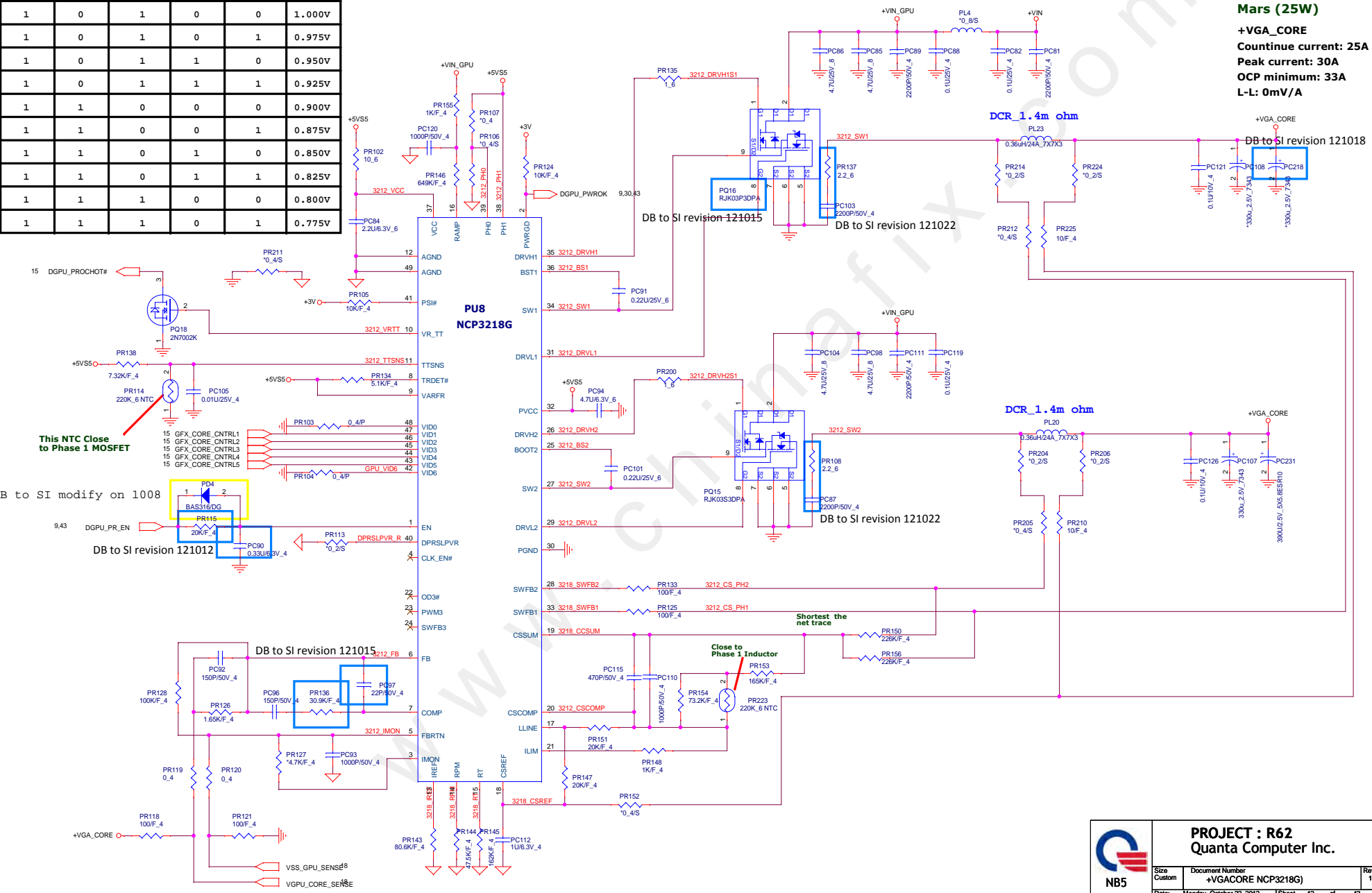






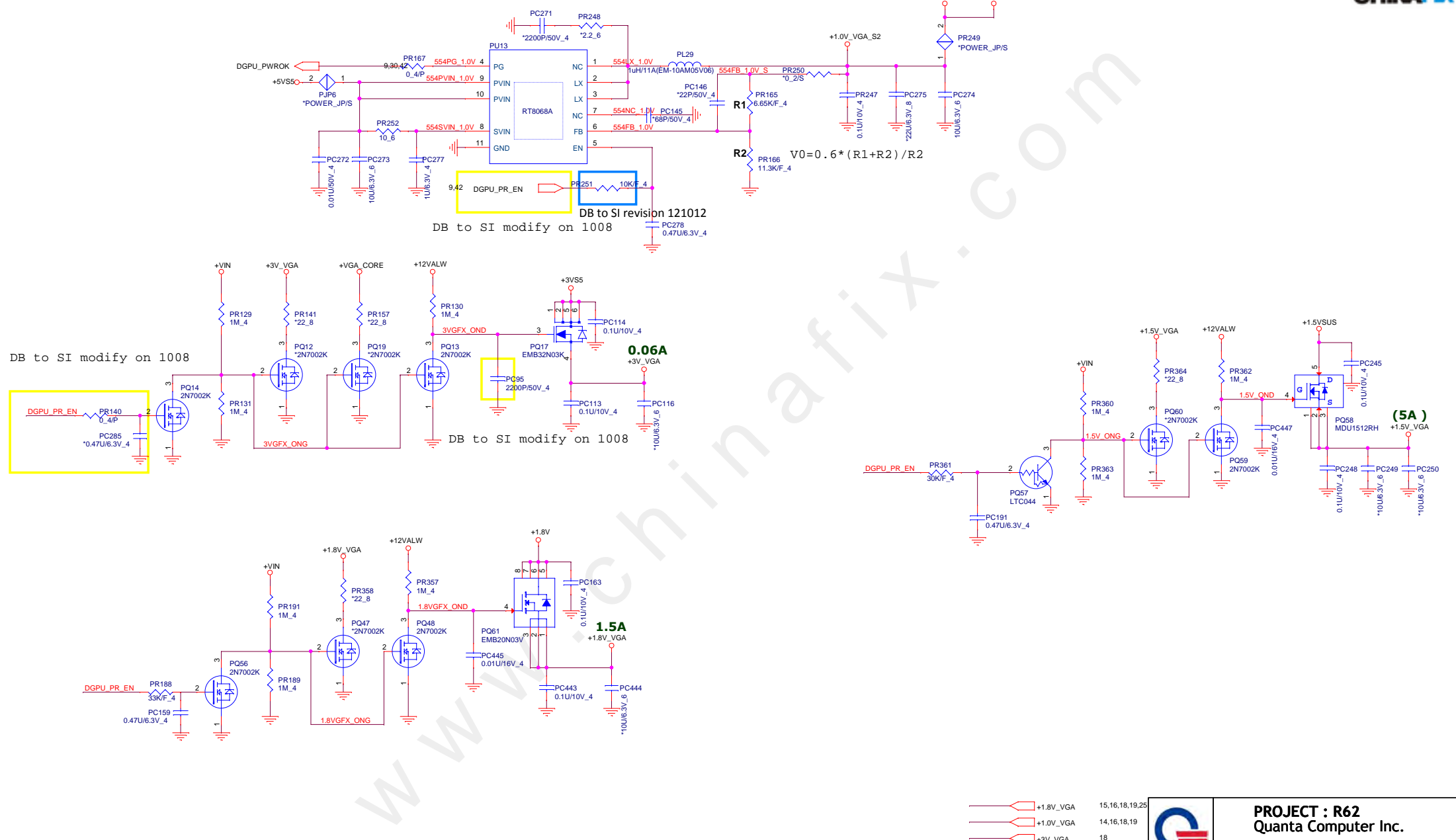
CHINAFOX


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Mars (25W)
+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

+0.95V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A



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